$$B1_{M_N} = 4^N B1_{M_N} - \sum_{n=0}^{N-1} 4^n$$

$$B2_{M_N} = \sum_{n=0}^{N} 4^n$$

; and

in a fourth row a third break point B3 of a third incrementation sequence is determined by the relationship

$$B3_{M_N} = 2 \times 4^N + 2$$

wherein M_N represents the memory of an Nth stage of said FFT processor.

8. The receiver according to claim 1, further comprising channel estimation and correction circuitry comprising:

pilot location circuitry receiving a transformed digital signal representing a frame from said FFT processor for locating pilot carriers therein, wherein said pilot carriers are spaced apart in a carrier spectrum of said transformed digital signal at intervals K and have predetermined magnitudes, said pilot location circuitry comprising:

a first circuit for computing an order of carriers in said transformed digital signal modulo K;

K accumulators coupled to said second circuit for accumulating magnitudes of said carriers in said transformed digital signal, said accumulated magnitudes defining a set; and

a correlation circuit for correlating K sets of accumulated magnitude values with said predetermined magnitudes, wherein a first member having a position calculated modulo K in each of said K sets is uniquely offset from a start position of said frame.

9. The receiver according to claim 8, wherein said pilot location circuitry further comprises a bit reversal circuit for reversing a bit order of said transformed digital signal.

10. The receiver according to claim 7, wherein said magnitudes of said carriers and said predetermined magnitudes are amplitudes.

11. The receiver according to claim 7, wherein said magnitudes of said carriers and said predetermined magnitudes are absolute values.

12. The receiver according to claim 7, wherein said correlation circuitry further comprises a peak tracking circuit for determining a spacing between a first peak and a second peak of said K sets of accumulated magnitudes.

13. The receiver according to claim 7, wherein said channel estimation and correction circuitry further comprises:

an interpolating filter for estimating a channel response between said pilot carriers; and

a multiplication circuit for multiplying data carriers output by said FFT processor with a correction coefficient produced by said interpolating filter.

14. The receiver according to claim 7, wherein said channel estimation and correction circuitry further comprises

a phase extraction circuit accepting a data stream of phase-uncorrected I and Q data from said FFT processor, and producing a signal representative of a phase angle of said uncorrected data, said phase extraction circuit including an accumulator for accumulating the phase angles of succeeding phase-uncorrected I and Q data.

15. The receiver according to claim 14, said channel estimation and correction circuitry further comprises:

an automatic frequency control circuit coupled to said phase extraction circuit and said accumulator, comprising;

a memory for storing an accumulated common phase error of a first symbol carried in said phase-uncorrected I and Q data;

wherein said accumulator is coupled to said memory and accumulates a difference between a common phase error of a plurality of pilot carriers in a second symbol and a common phase error of corresponding pilot carriers in said first symbol;

an output of said accumulator being coupled to said I/Q demodulator.

16. The receiver according to claim 15, wherein said coupled output of said accumulator is enabled in said I/Q demodulator only during reception of a guard interval therein.

17. The receiver according to claim 14, said channel estimation and correction circuitry further comprises an automatic sampling rate control circuit coupled to said phase extraction circuit, comprising:

a memory for storing accumulated phase errors of pilot carriers in a first symbol carried in said phase-uncorrected I and Q data;

wherein said accumulator is coupled to said memory and accumulates differences between phase errors of pilot carriers in a second symbol and phase errors of corresponding pilot carriers in said first symbol to define a plurality of accumulated intersymbol carrier phase error differentials, a phase slope being defined by a difference between a first accumulated intersymbol carrier phase differential and a second accumulated intersymbol carrier phase differential;

an output of said accumulator being coupled to said I/Q demodulator.

18. The receiver according to claim 17, wherein said sampling rate control circuit stores a plurality of accumulated intersymbol carrier phase error differentials and computes a line of best fit therebetween.

19. The receiver according to claim 17, wherein said coupled output signal of said accumulator is enabled in said resampling circuit only during reception of a guard interval therein.

20. The receiver according to claim 17, wherein a common memory for storing output of said phase extraction circuit is coupled to said automatic frequency control circuit and to said automatic sampling rate control circuit.

21. The receiver according to claim 14, wherein said phase extraction circuit further comprises:

a pipelined circuit for iteratively computing the arctangent of an angle of rotation according to the series

$$\tan^{-1}(x) = x - \frac{x^3}{3} + \frac{x^5}{5} - \frac{x^7}{7} + \frac{x^9}{9} - \ldots, \qquad |x| < 1$$

wherein x is a ratio of said phase-uncorrected I and Q data.

22. The receiver according to claim 21, wherein said pipelined circuit comprises:

a constant coefficient multiplier; and

a multiplexer for selecting one of a plurality of constant coefficients of said series, an output of said multiplexer being connected to an input of said constant coefficient multiplier.

23. The receiver according to claim 21, wherein said pipelined circuit comprises:

a multiplier;

a first memory for storing the quantity x^2, said first memory being coupled to a first input of said multiplier;

a second memory for holding an output of said multiplier; and

a feedback connection between said second memory and a second input of said multiplier.

24. The receiver according to claim 21, wherein said pipelined circuit further comprises:

a third memory for storing a value of said series;

a control circuit, coupled to said third memory, wherein said pipeline circuit computes N terms of said series, and said pipeline circuit computes N+1 terms of said series, wherein N is an integer;

an averaging circuit coupled to said third memory for computing an average of said N terms and said N+1 terms of said series.

25. The receiver according to claim 1, wherein data transmitted in a pilot carrier of said multicarrier signal is BCH encoded according to a code generator polynomial h(x), further comprising:

a demodulator operative on said BCH encoded data;

an iterative pipelined BCH decoding circuit, comprising:

a circuit coupled to said demodulator for forming a Galois Field of said polynomial, and calculating a plurality of syndromes therewith;

a plurality of storage registers, each said storage register storing a respective one of said syndromes;

a plurality of feedback shift registers, each said feedback shift register accepting data from a respective one of said storage registers and having an output;

a plurality of Galois field multipliers, each said multiplier being connected in a feedback loop across a respective one of said feedback shift registers and multiplying the output of its associated feedback shift register by an alpha value of said Galois Field;

an output Galois field multiplier for multiplying said outputs of two of said feedback shift registers;

an error detection circuit connected to said feedback shift registers and said output Galois field multiplier, wherein an ouput signal of said error detection circuit indicates an error in a current bit of data; and

a feedback line enabled by said error detection circuit and connected to said storage registers, wherein outputs of said feedback shift registers are written into said storage registers.

26. The receiver according to claim 25, wherein said output Galois field multiplier comprises:

a first register initially storing a first multiplicand A;

a constant coefficient multiplier connected to said register for multiplication by a value α, an output of said constant coefficient multiplier being connected to said first register to define a first feedback loop, whereby in a kth cycle of clocked operation said first register contains a Galois field product $A\alpha^k$;

a second register for storing a second multiplicand B;

an AND gate connected to said second register and to said output of said constant coefficient multiplier;

an adder having a first input connected to an output of said AND gate;

an accumulator connected to a second input of said adder; wherein an output of said adder is connected to said accumulator to define a second feedback loop; whereby a Galois field product AB is output by said adder.

27. A method for estimation of a frequency response of a channel, comprising the steps of:

receiving from a channel a multicarrier signal having a plurality of data carriers and scattered pilot carriers, said scattered pilot carriers being spaced apart at a first interval N and being transmitted at a power that differs from a transmitted power of said data carriers;

converting said multicarrier signal to a digital representation thereof;

performing a Fourier transform on said digital representation of said multicarrier signal to generate a transformed digital signal;

reversing a bit order of said transformed digital signal to generate a bit-order reversed signal;

cyclically accumulating magnitudes of carriers in said bit-order reversed signal in N accumulators;

correlating said accumulated magnitudes with said power of said scattered pilot carriers;

responsive to said step of correlating, generating a synchronizing signal that identifies a carrier of said multicarrier signal.

28. The method according to claim 27, wherein said step of accumulating magnitudes comprises the steps of:

adding absolute values of a real component of said bit-order reversed signal to respective absolute values of imaginary components thereof to generate sums;

respectively storing said sums in said accumulators.

29. The method according to claim 27, wherein said step of correlating said accumulated magnitudes further comprises the step of:

identifying a first accumulator having a highest value stored therein representing a first carrier position.

30. The method according to claim 29, wherein said step of correlating said accumulated magnitudes further comprises the steps of:

identifying a second accumulator having a second highest value stored therein representing a second carrier position; and

determining an interval between said first carrier position and said second carrier position.

31. The method according to claim 27, further comprising the steps of:

comparing a position of a carrier of a first symbol in said bit-order reversed signal with a position of a carrier of a second symbol therein.

32. The method according to claim 27, further comprising the steps of:

interpolating between pilot carriers to determine correction factors for respective intermediate data carriers disposed therebetween; and

respectively adjusting magnitudes of said intermediate data carriers according to said correction factors.

33. The method according to claim 27, further comprising the steps of:

determining a mean phase difference between corresponding pilot carriers of successive symbols being transmitted in said transformed digital signal; and

generating a first control signal responsive to said mean phase difference; and

responsive to said first control signal adjusting a frequency of reception of said multicarrier signal.

34. The method according to claim 33, further comprising the steps of:

determining a first phase difference between a first data carrier of a first symbol in said transmitted data carrier and said first data carrier of a second symbol therein;

determining a second phase difference between a second data carrier of said first symbol and said second data carrier of said second symbol; and

determining a difference between said first phase difference and said second phase difference to define a phase slope between said first data carrier and said second data carrier;

generating a second control signal responsive to said phase slope; and

responsive to said second control signal adjusting a sampling frequency of said multicarrier signal.

35. The method according to claim 34, wherein said step of determining a difference between said first phase difference and said second phase difference comprises computing a line of best fit.

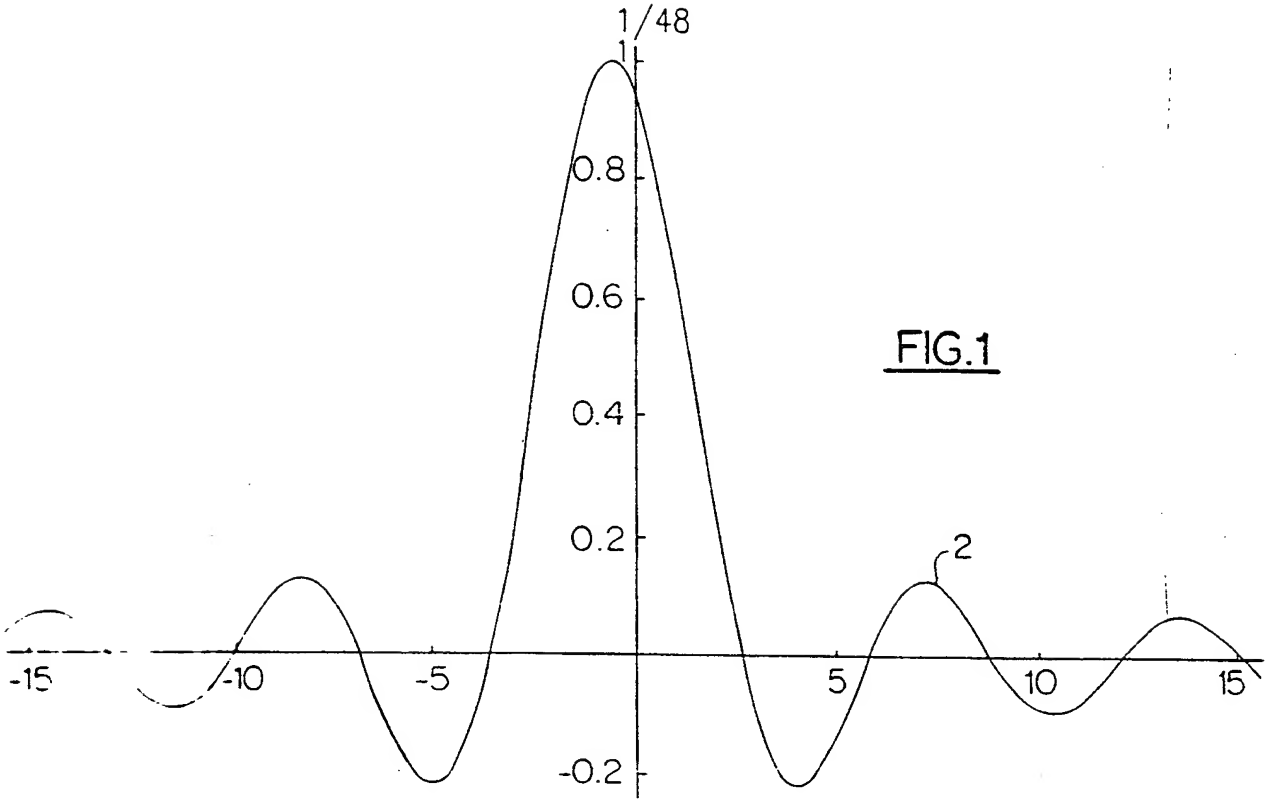


FIG.1

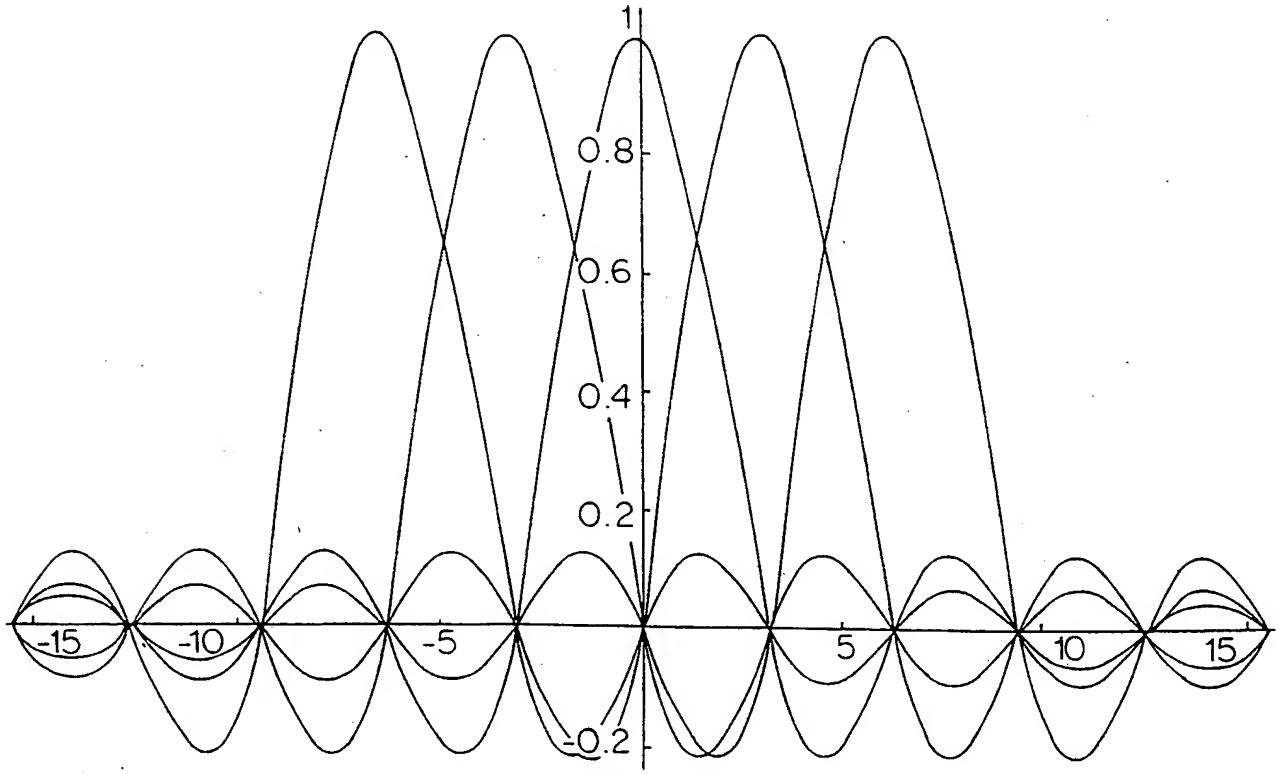


FIG.2

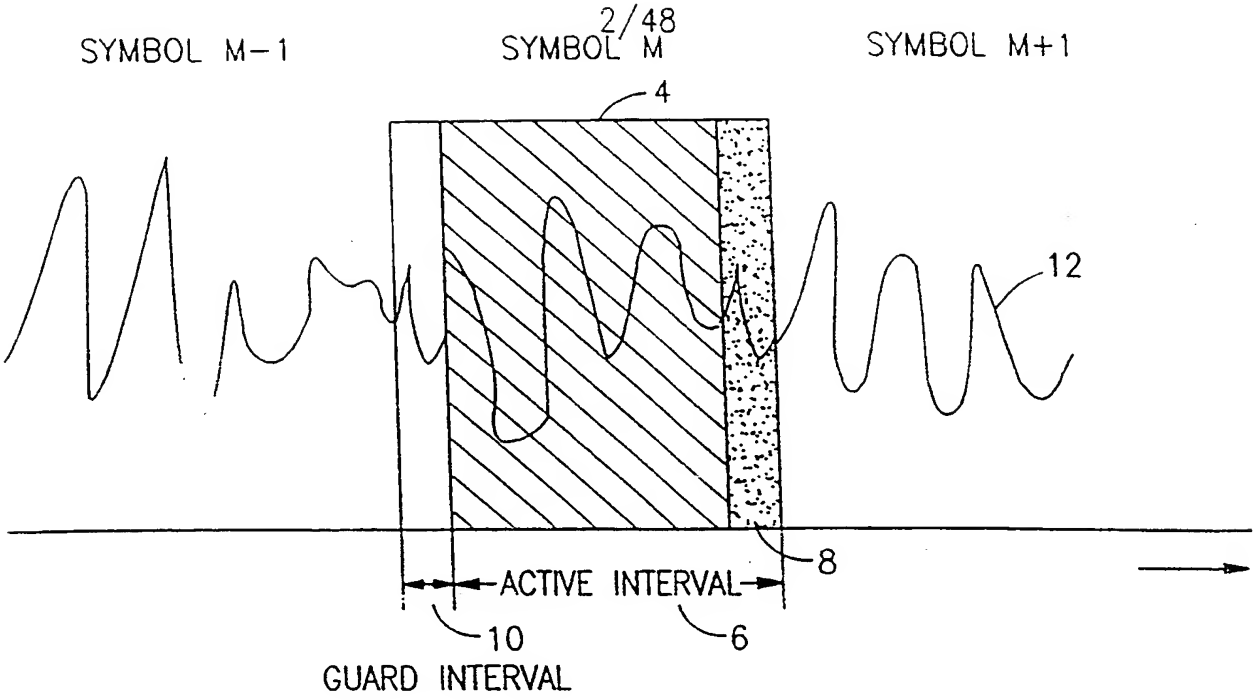

SYMBOL M-1
SYMBOL M
SYMBOL M+1
4
12
8
ACTIVE INTERVAL
10
6
GUARD INTERVAL

FIG.3

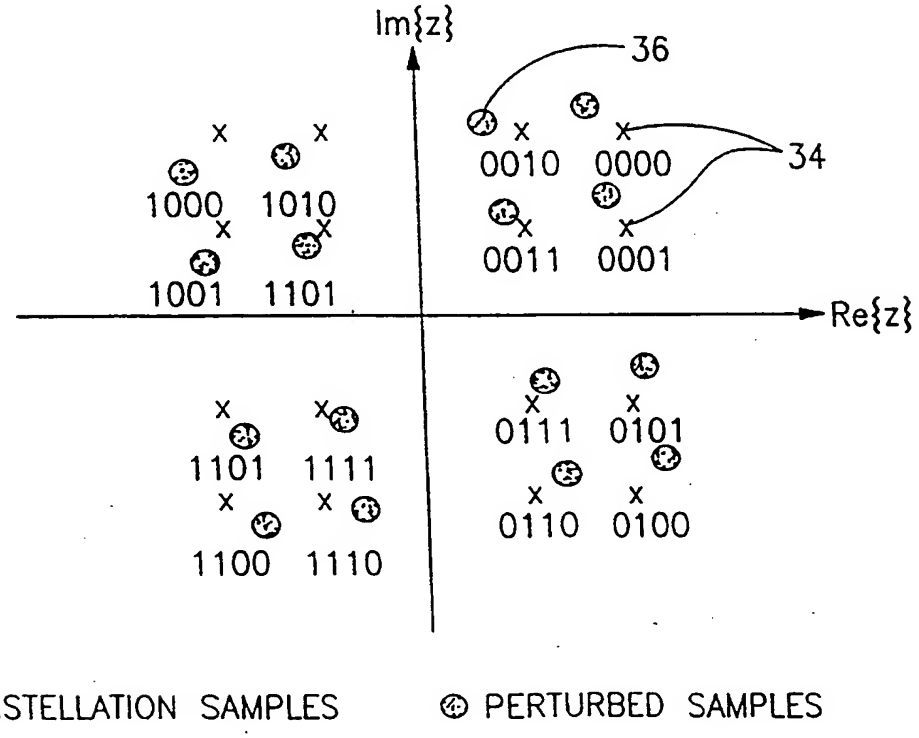

Im{z}
36
34
0010
0000
0011
0001
1000
1010
1001
1101
Re{z}
0111
0101
0110
0100
1101
1111
1100
1110
X IDEAL CONSTELLATION SAMPLES
PERTURBED SAMPLES

FIG.5

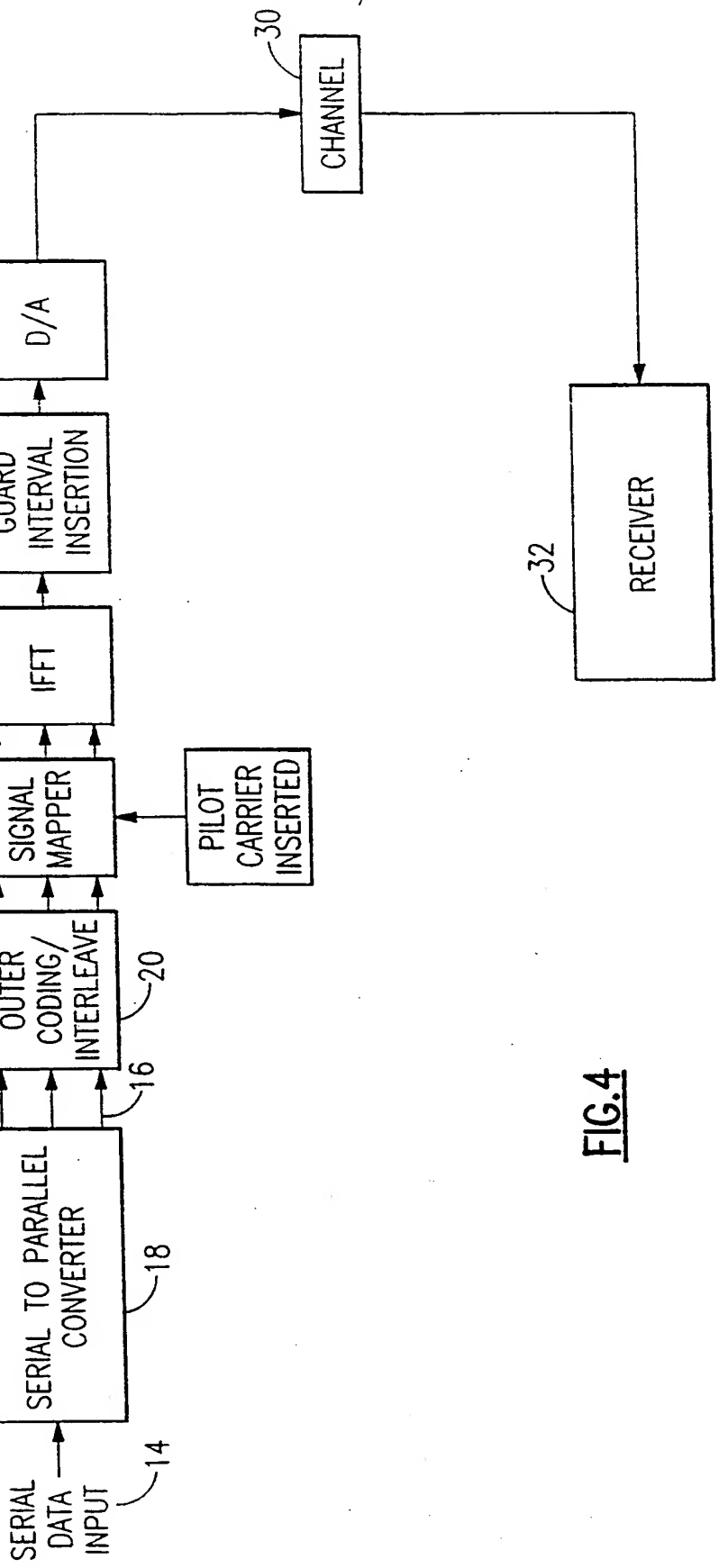

SERIAL DATA INPUT
14
SERIAL TO PARALLEL CONVERTER
18
16
OUTER CODING/ INTERLEAVE
20
SIGNAL MAPPER
22
PILOT CARRIER INSERTED
IFFT
24
GUARD INTERVAL INSERTION
26
D/A
28
CHANNEL
30
RECEIVER
32

FIG.4

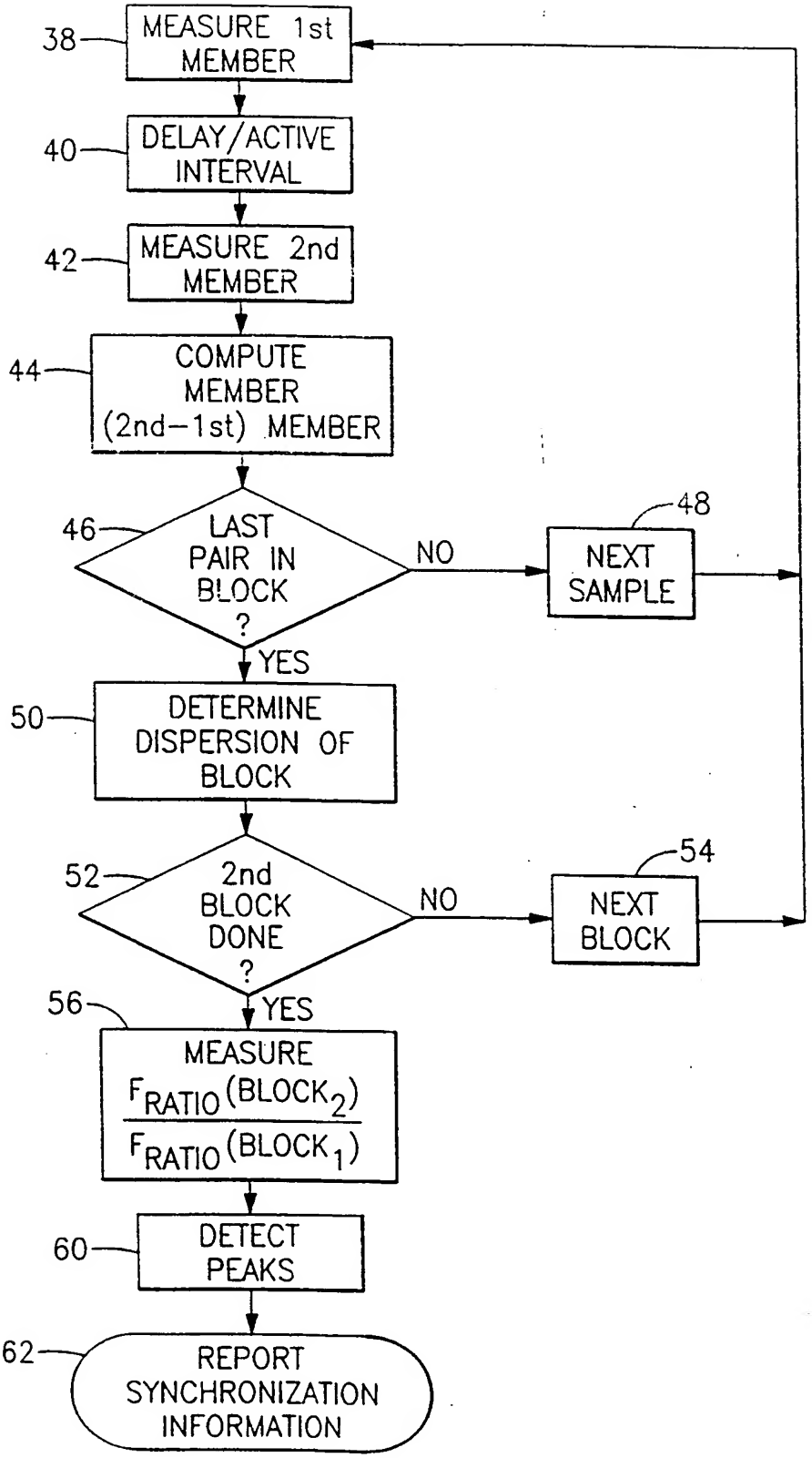


FIG.6

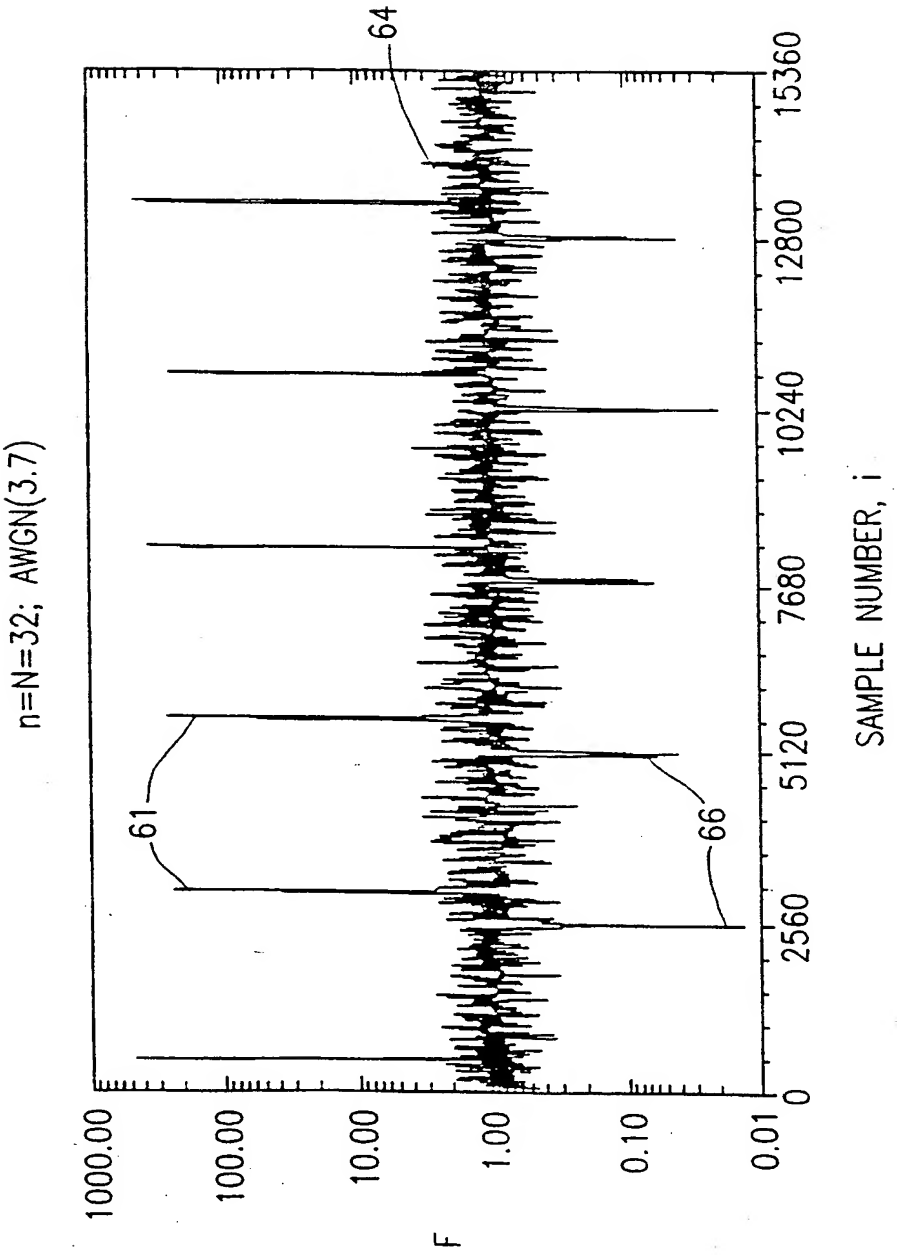


FIG.7

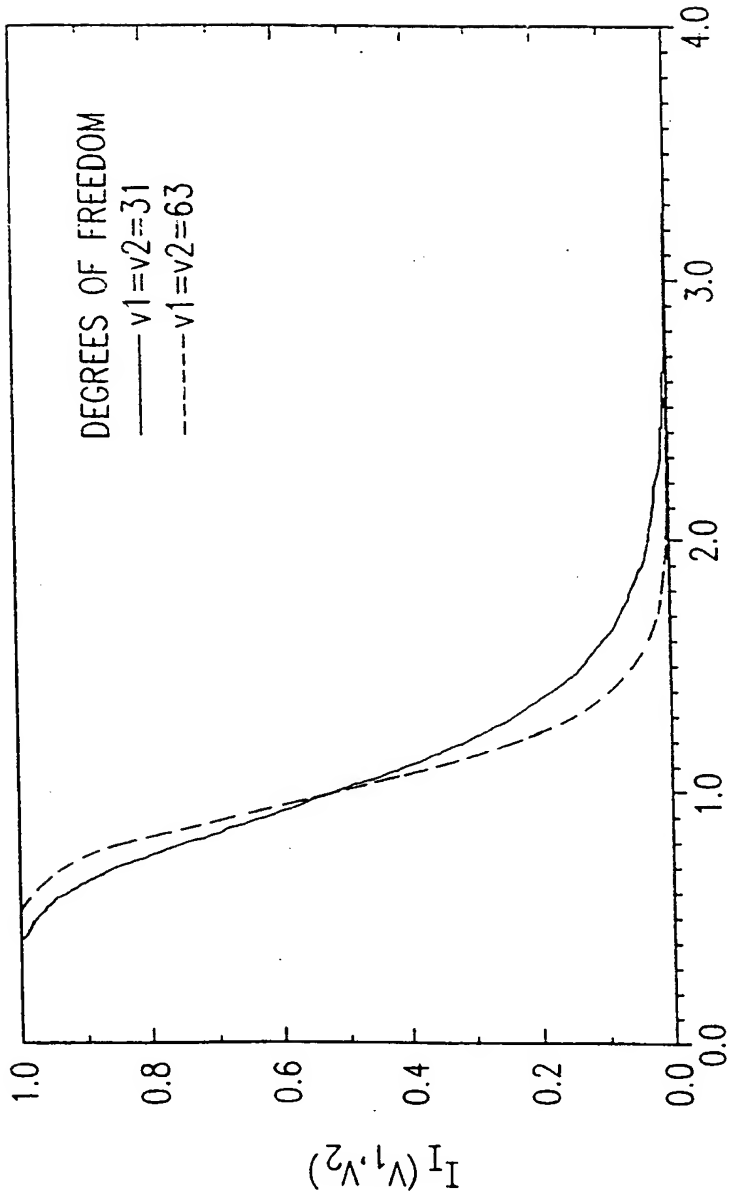

DEGREES OF FREEDOM
v1=v2=31
v1=v2=63
$I_I(v_1,v_2)$
1.0
0.8
0.6
0.4
0.2
0.0
0.0
1.0
2.0
3.0
4.0
RATIO OF VARIANCES, F

FIG.8

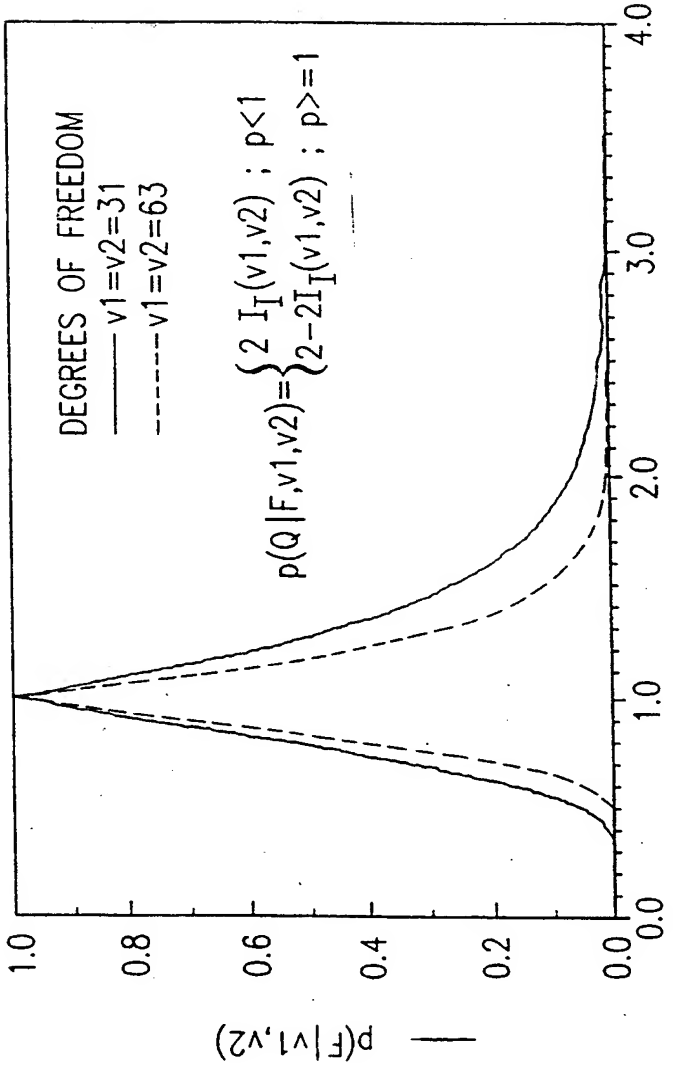


FIG.9

$$y/2 = \frac{\sum_{0}^{N-1} |S_{i-j}|}{\sum_{0}^{N-1} |S_{i-n-j}|}$$

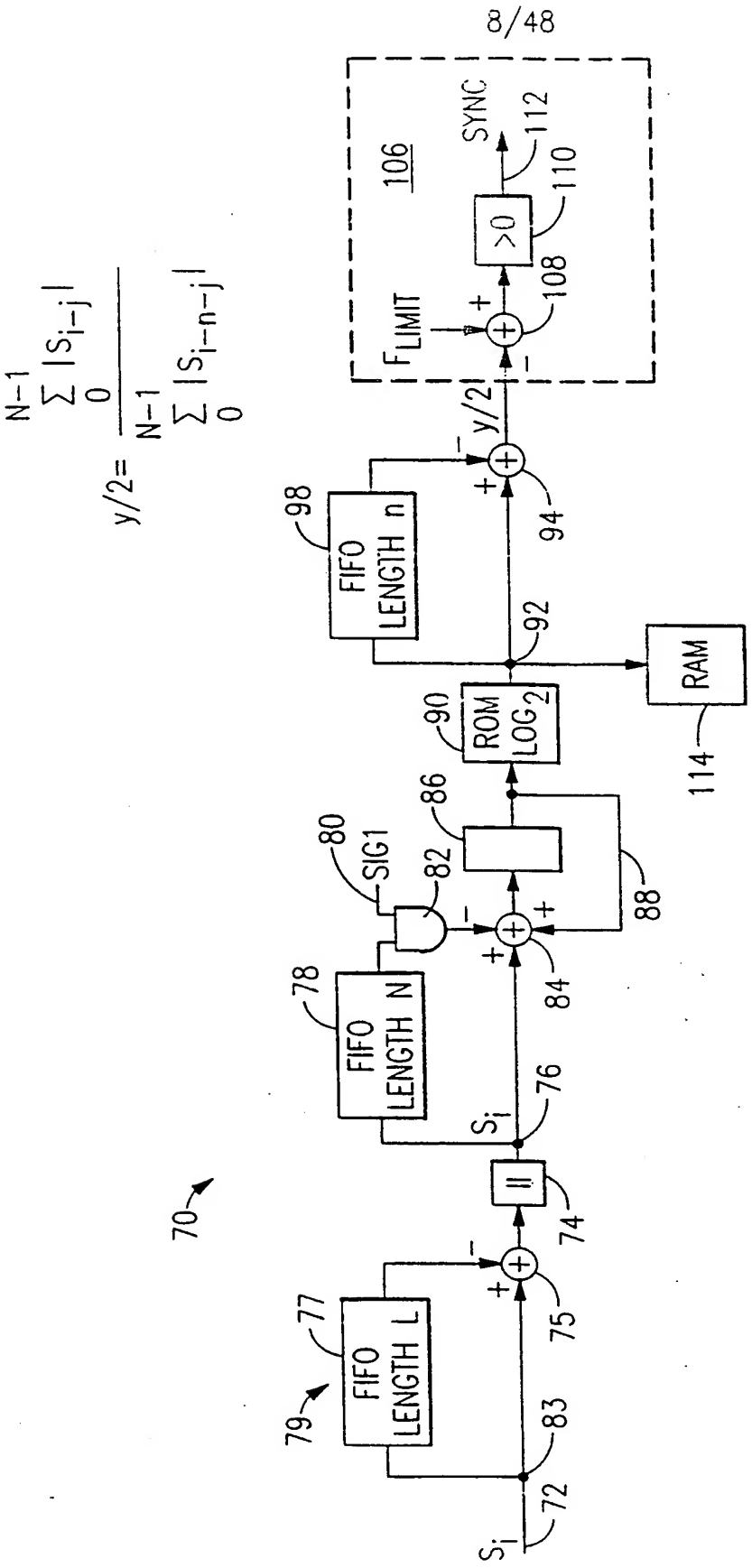


FIG.10

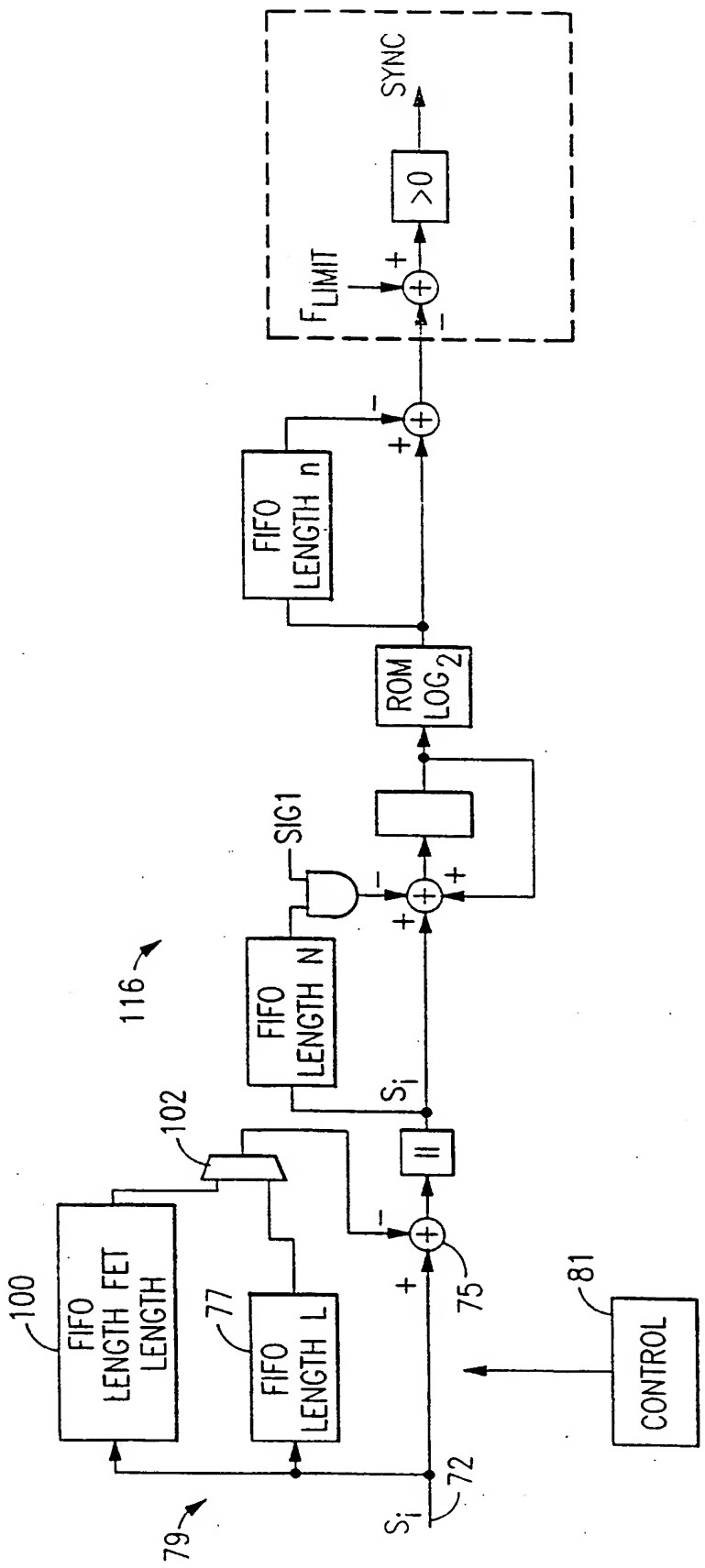


FIG.11

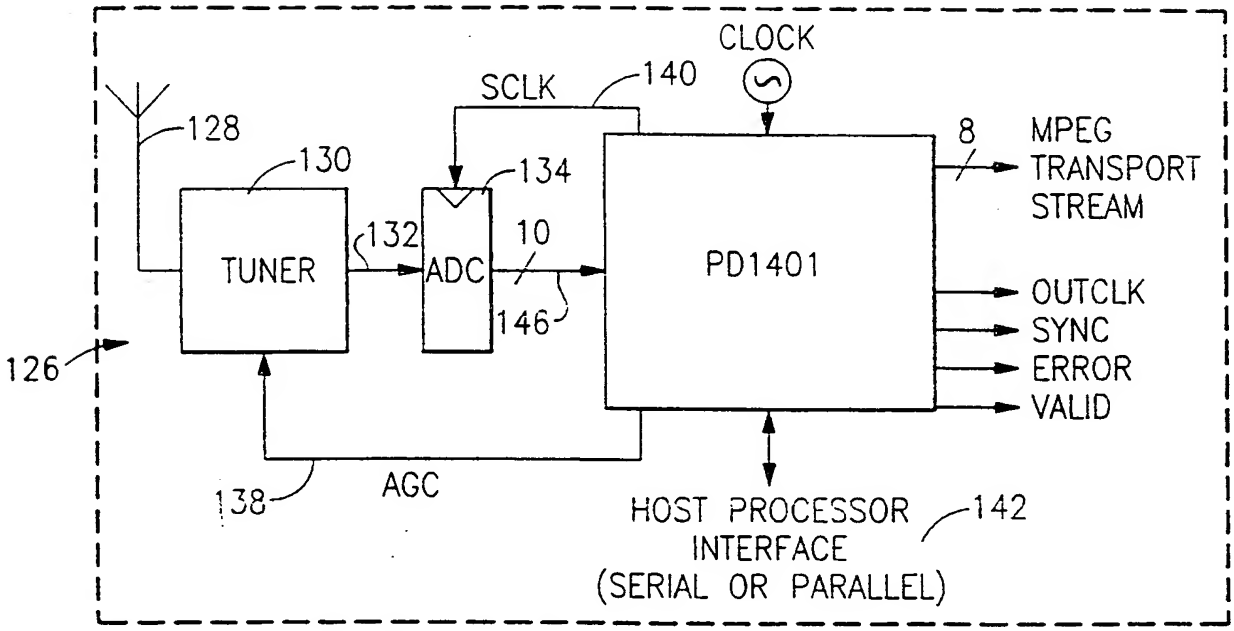


FIG.12

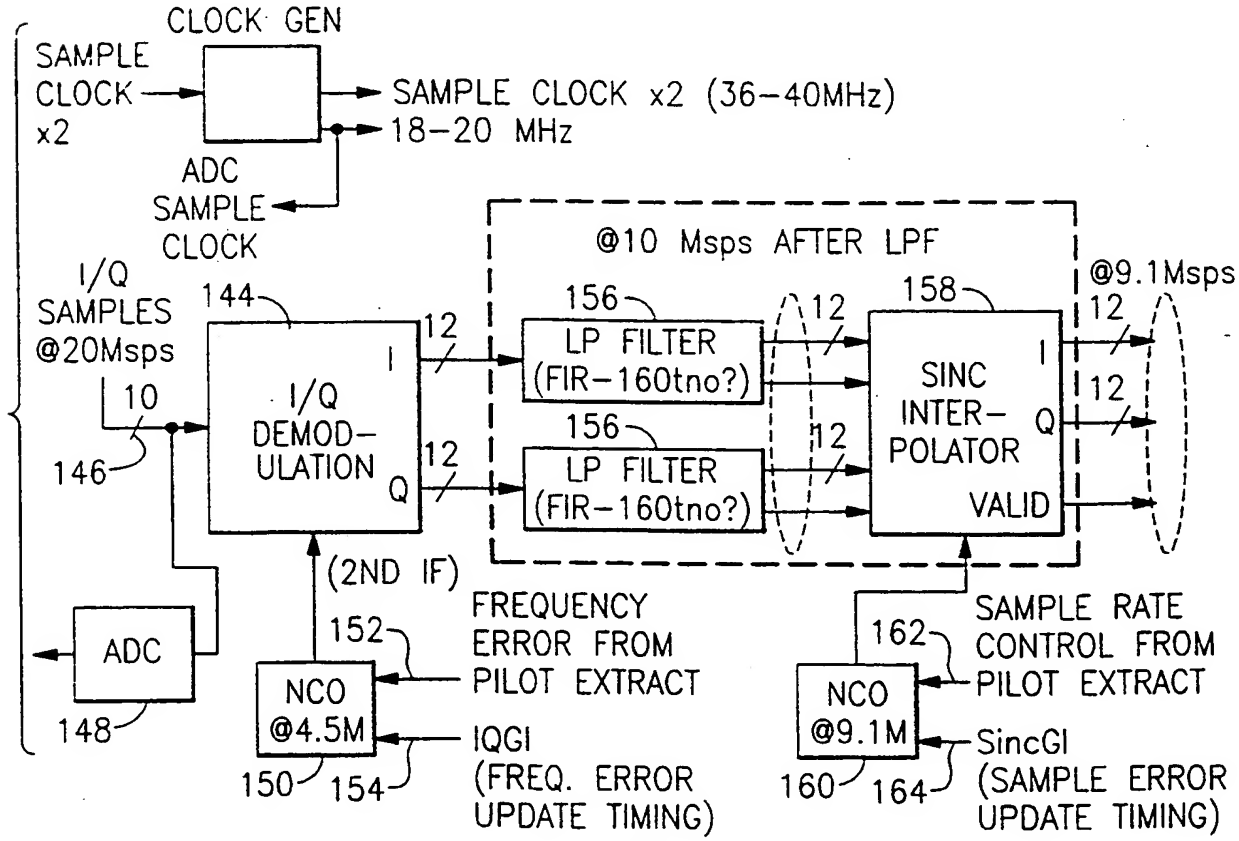


FIG.13

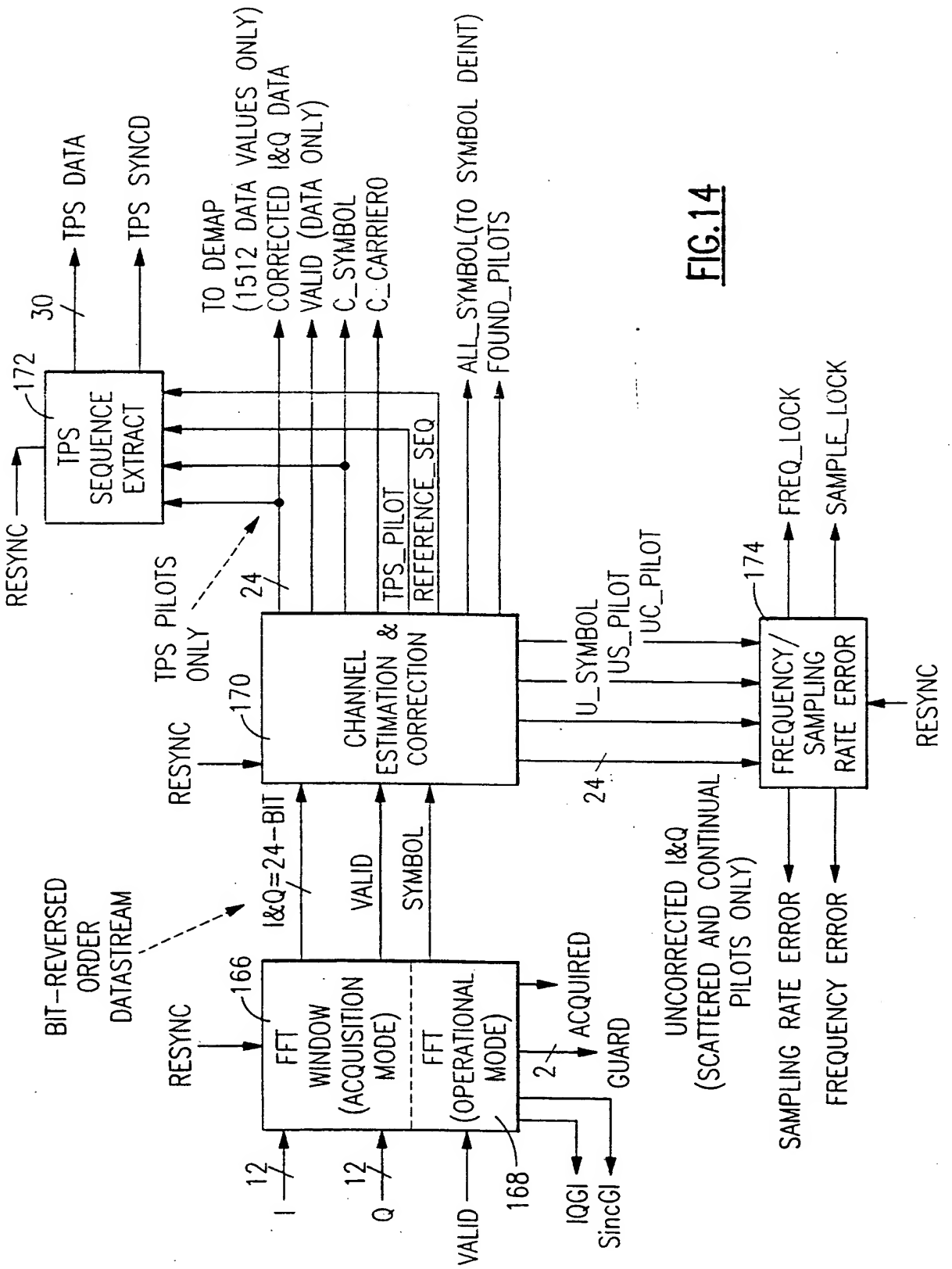

TPS DATA
TPS SYNCD
30
172
TPS SEQUENCE EXTRACT
RESYNC
TO DEMAP (1512 DATA VALUES ONLY)
CORRECTED I&Q DATA
VALID (DATA ONLY)
C_SYMBOL
C_CARRIER0
TPS_PILOT REFERENCE_SEQ
ALL_SYMBOL(TO SYMBOL DEINT)
FOUND_PILOTS
TPS PILOTS ONLY
24
RESYNC
170
CHANNEL ESTIMATION & CORRECTION
U_SYMBOL
US_PILOT
UC_PILOT
174
FREQ_LOCK
SAMPLE_LOCK
FREQUENCY/ SAMPLING RATE ERROR
RESYNC
BIT-REVERSED ORDER DATASTREAM
I&Q=24-BIT
VALID
SYMBOL
24
UNCORRECTED I&Q (SCATTERED AND CONTINUAL PILOTS ONLY)
RESYNC
166
FFT WINDOW (ACQUISITION MODE)
FFT (OPERATIONAL MODE)
2
ACQUIRED
GUARD
12
I
12
Q
VALID
168
IQGI
SincGI
SAMPLING RATE ERROR
FREQUENCY ERROR

FIG.14

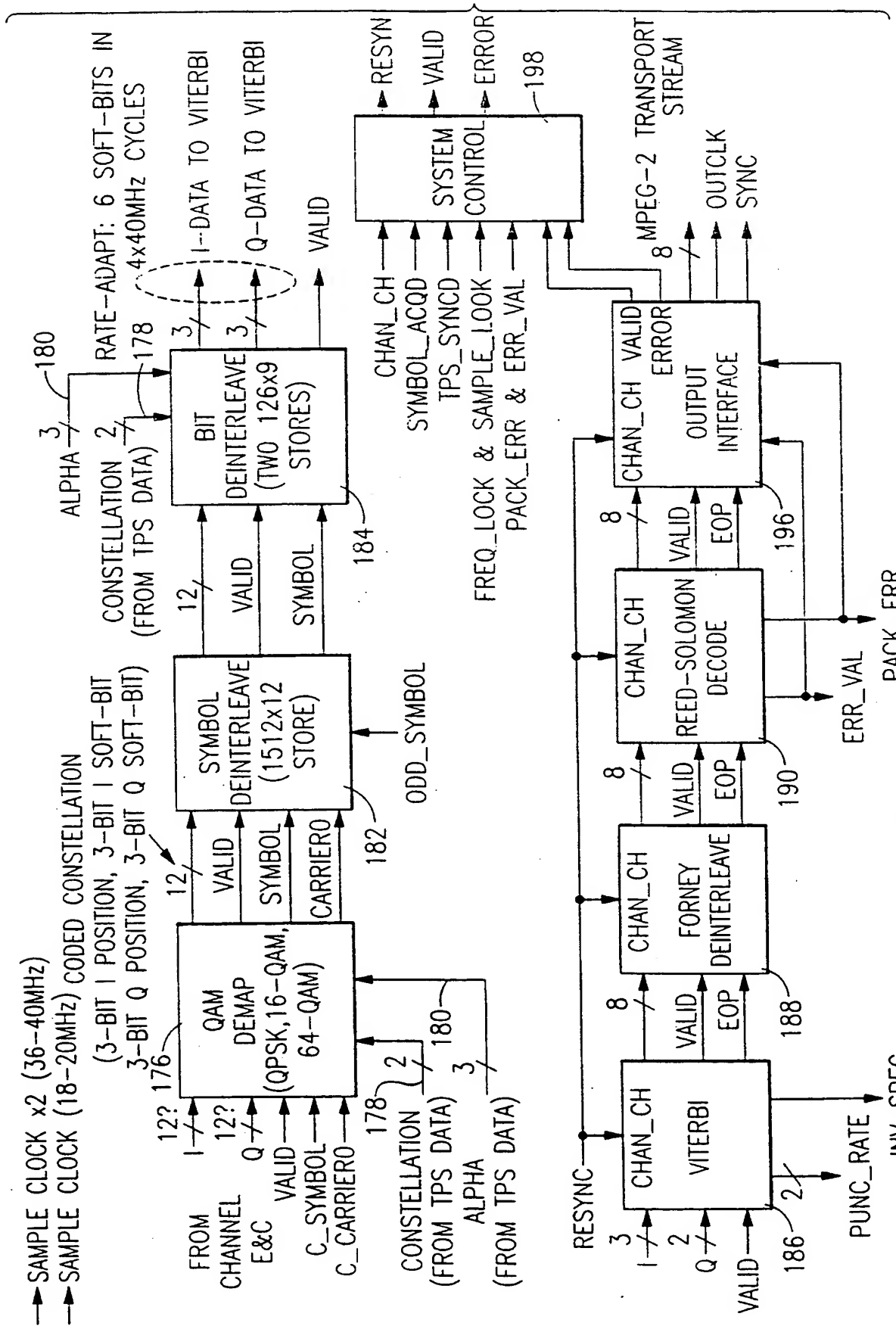


FIG.15

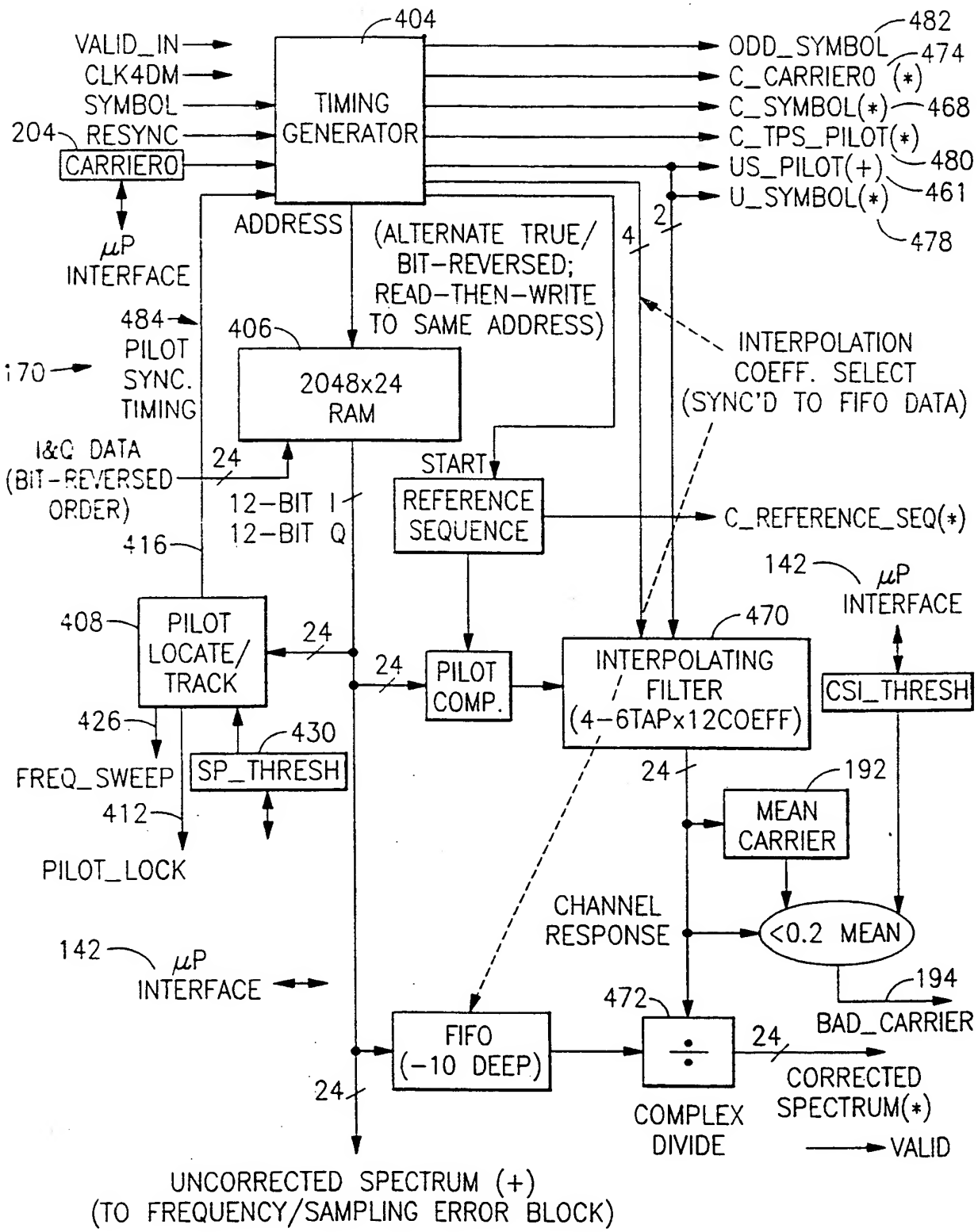

404
VALID_IN
CLK4DM
SYMBOL
204
RESYNC
CARRIER0
TIMING GENERATOR
ODD_SYMBOL
482
474
C_CARRIER0 (*)
C_SYMBOL(*)
468
C_TPS_PILOT(*)
US_PILOT(+)
480
U_SYMBOL(*)
461
478
μP INTERFACE
ADDRESS
(ALTERNATE TRUE/ BIT-REVERSED; READ-THEN-WRITE TO SAME ADDRESS)
4
2
484
406
170
PILOT SYNC. TIMING
2048x24 RAM
INTERPOLATION COEFF. SELECT (SYNC'D TO FIFO DATA)
I&Q DATA (BIT-REVERSED ORDER)
24
START
12-BIT I
12-BIT Q
REFERENCE SEQUENCE
C_REFERENCE_SEQ(*)
416
142
μP INTERFACE
408
PILOT LOCATE/ TRACK
24
24
PILOT COMP.
470
INTERPOLATING FILTER (4-6TAPx12COEFF)
CSI_THRESH
426
430
FREQ_SWEEP
SP_THRESH
24
192
412
MEAN CARRIER
PILOT_LOCK
CHANNEL RESPONSE
<0.2 MEAN
142
μP INTERFACE
194
BAD_CARRIER
472
FIFO (-10 DEEP)
24
24
CORRECTED SPECTRUM(*)
COMPLEX DIVIDE
VALID
UNCORRECTED SPECTRUM (+)
(TO FREQUENCY/SAMPLING ERROR BLOCK)

FIG.16

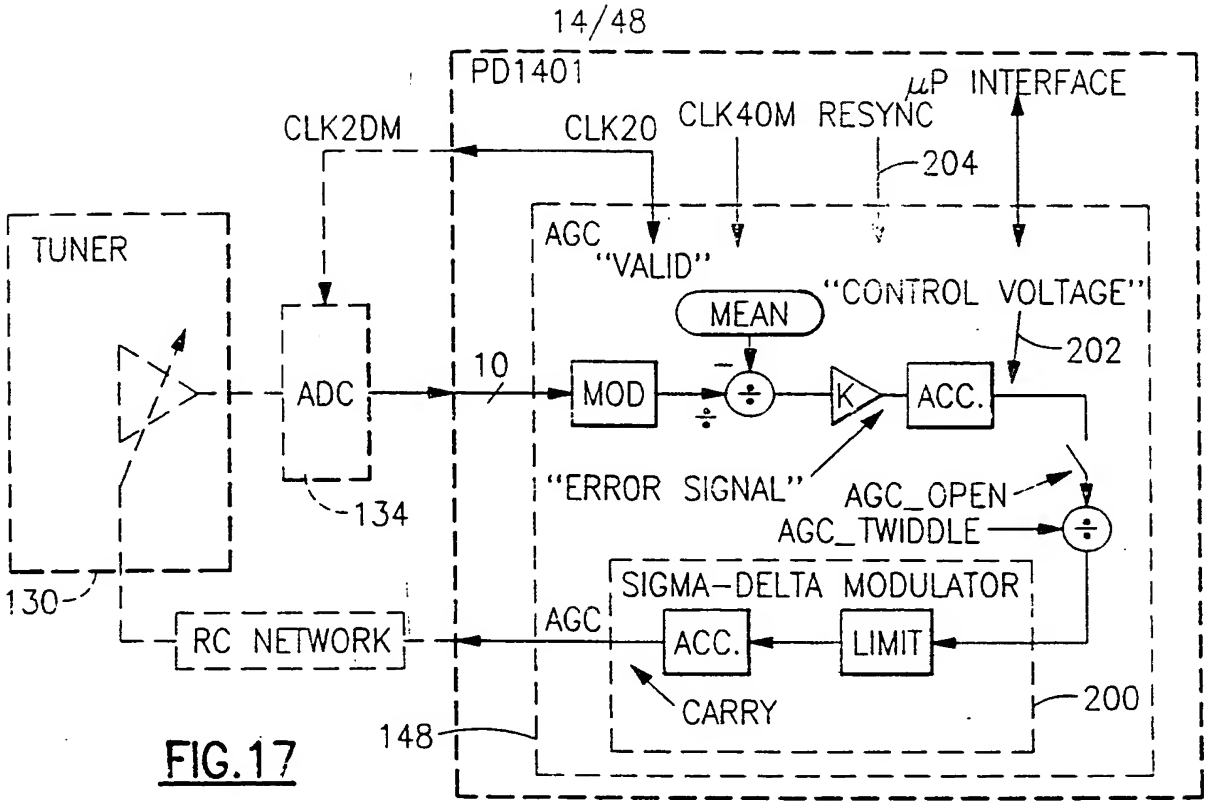

PD1401
μP INTERFACE
CLK2DM
CLK20
CLK40M
RESYNC
204
TUNER
AGC
"VALID"
MEAN
"CONTROL VOLTAGE"
202
ADC
10
MOD
K
ACC.
"ERROR SIGNAL"
AGC_OPEN
AGC_TWIDDLE
134
130
SIGMA-DELTA MODULATOR
AGC
RC NETWORK
ACC.
LIMIT
CARRY
200
148

FIG.17

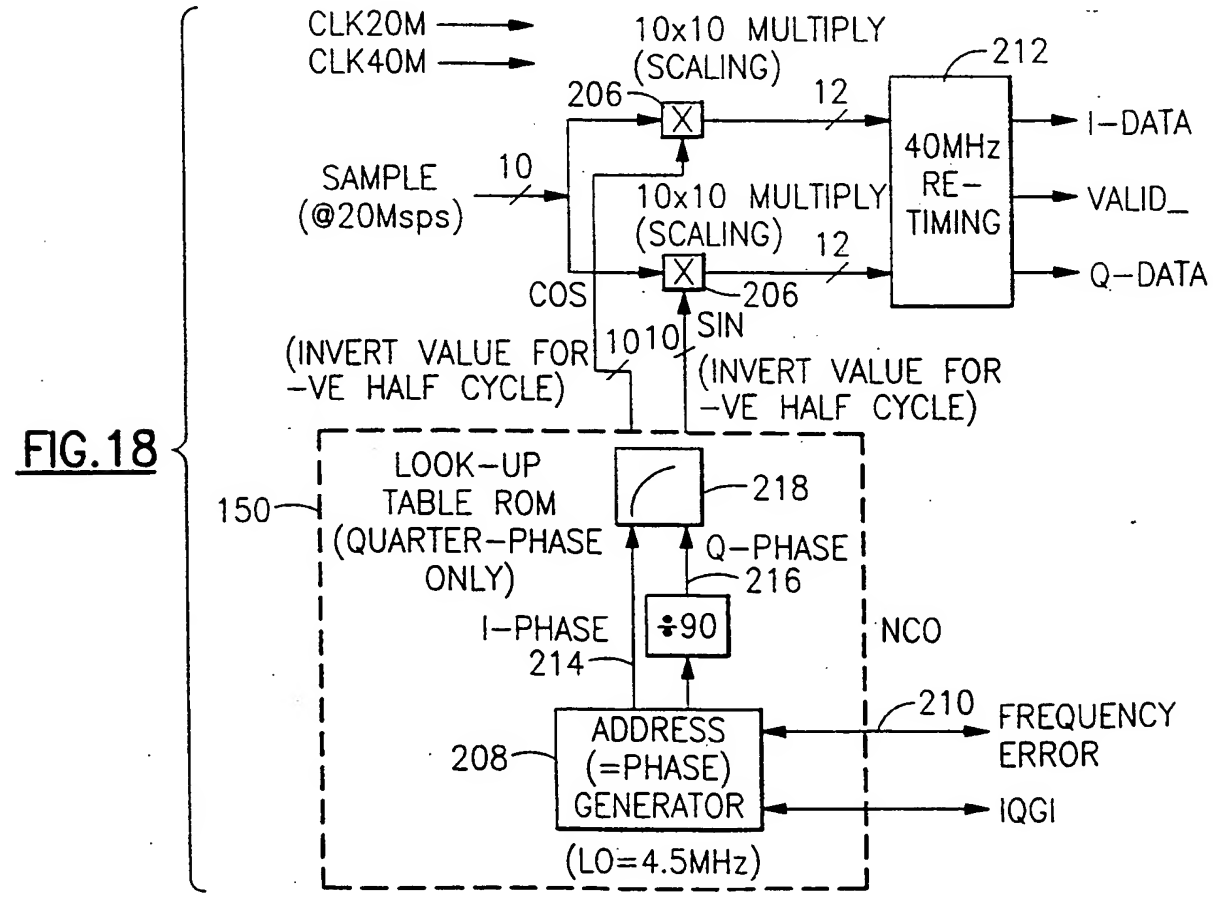

CLK20M
CLK40M
10x10 MULTIPLY
(SCALING)
212
206
12
I-DATA
SAMPLE
(@20Msps)
10
10x10 MULTIPLY
(SCALING)
40MHz
RE-
TIMING
VALID_
12
Q-DATA
COS
206
SIN
(INVERT VALUE FOR
-VE HALF CYCLE)
1010
(INVERT VALUE FOR
-VE HALF CYCLE)
LOOK-UP
TABLE ROM
(QUARTER-PHASE
ONLY)
150
218
Q-PHASE
216
I-PHASE
214
÷90
NCO
210
FREQUENCY
ERROR
208
ADDRESS
(=PHASE)
GENERATOR
IQGI
(LO=4.5MHz)

FIG.18

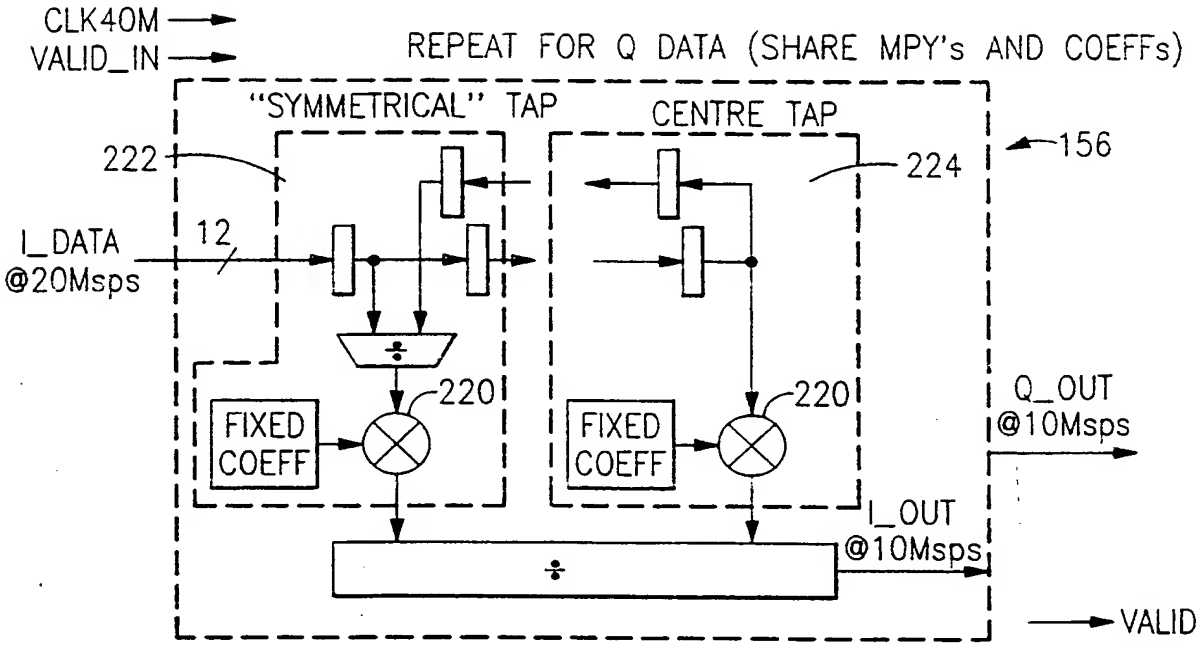

CLK40M
VALID_IN
REPEAT FOR Q DATA (SHARE MPY's AND COEFFs)
"SYMMETRICAL" TAP
CENTRE TAP
156
222
224
I_DATA
@20Msps
12
220
220
FIXED
COEFF
FIXED
COEFF
Q_OUT
@10Msps
I_OUT
@10Msps
VALID

FIG.19

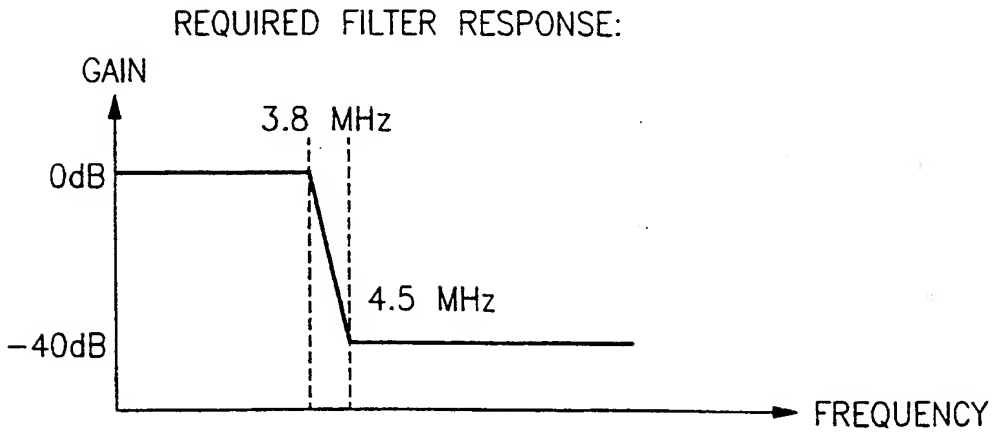

REQUIRED FILTER RESPONSE:
GAIN
3.8 MHz
0dB
4.5 MHz
-40dB
FREQUENCY

FIG.20

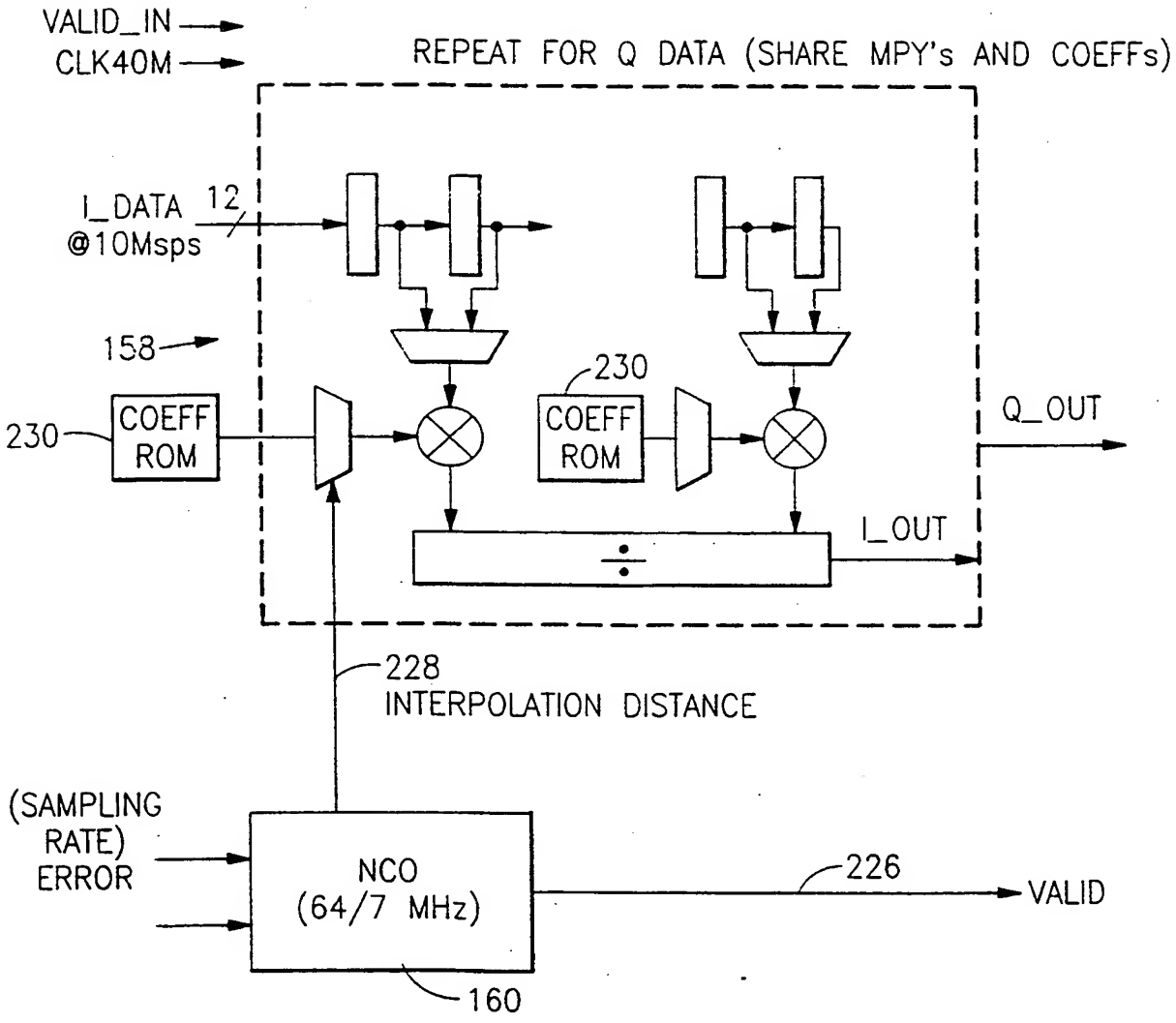

VALID_IN
CLK40M
REPEAT FOR Q DATA (SHARE MPY's AND COEFFs)
I_DATA 12
@10Msps
158
230
COEFF ROM
230
COEFF ROM
Q_OUT
I_OUT
228
INTERPOLATION DISTANCE
(SAMPLING RATE) ERROR
NCO (64/7 MHz)
226
VALID
160

FIG.21

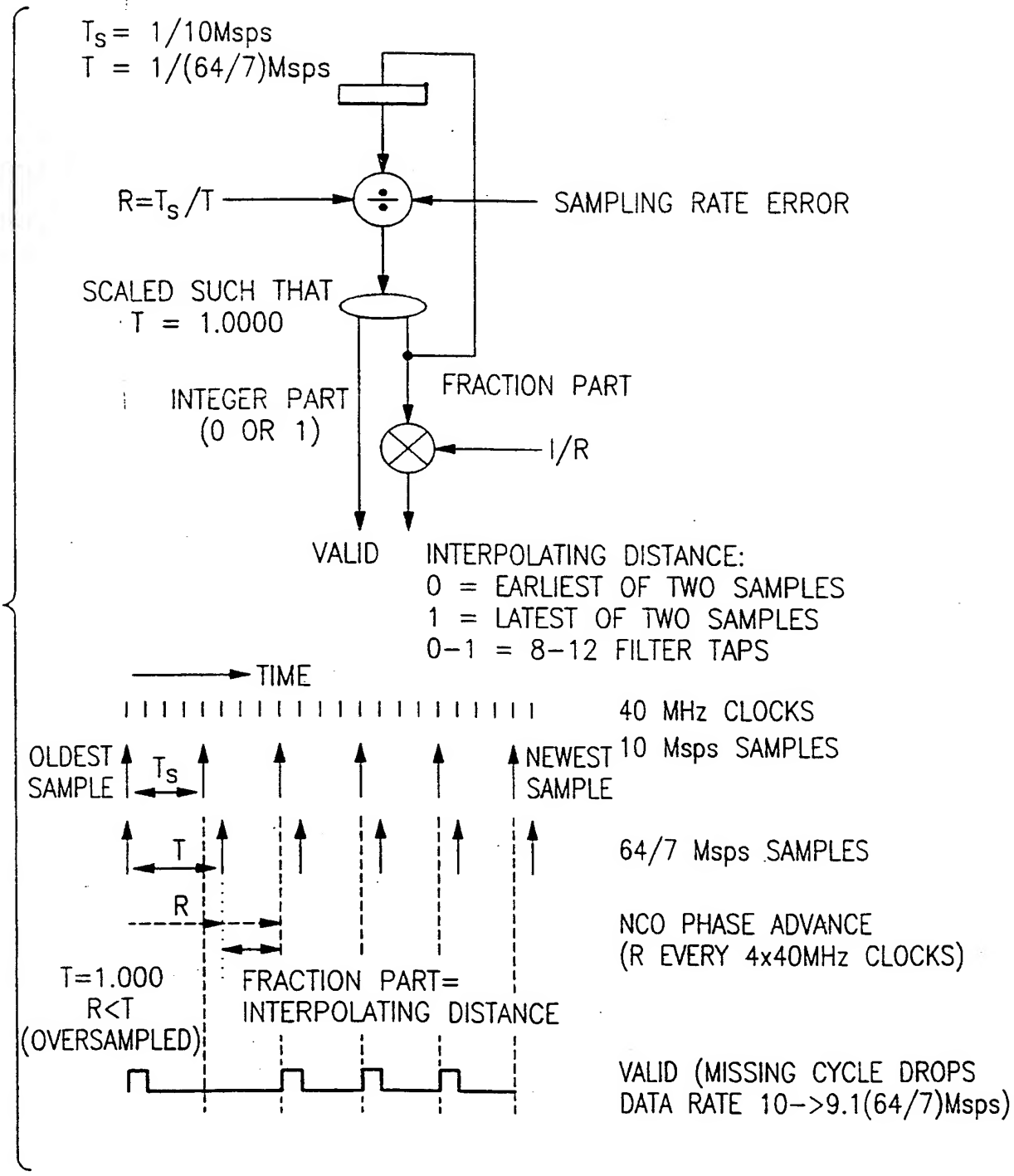


FIG.22

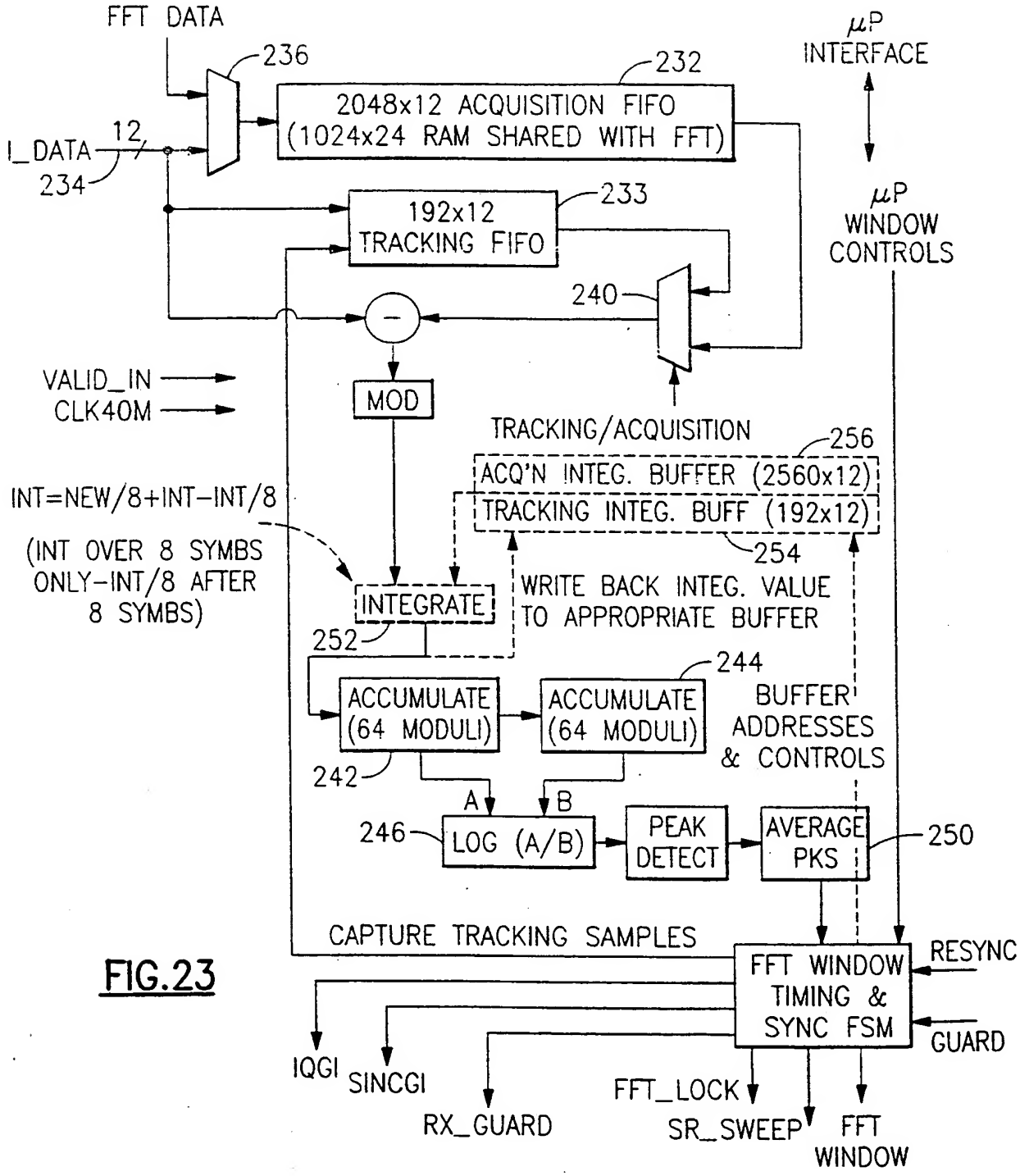

FFT DATA
236
232
μP INTERFACE
2048x12 ACQUISITION FIFO (1024x24 RAM SHARED WITH FFT)
I_DATA
12
234
192x12 TRACKING FIFO
233
μP WINDOW CONTROLS
240
VALID_IN
CLK40M
MOD
TRACKING/ACQUISITION
256
ACQ'N INTEG. BUFFER (2560x12)
TRACKING INTEG. BUFF (192x12)
254
INT=NEW/8+INT-INT/8
(INT OVER 8 SYMBS ONLY-INT/8 AFTER 8 SYMBS)
INTEGRATE
WRITE BACK INTEG. VALUE TO APPROPRIATE BUFFER
252
244
ACCUMULATE (64 MODULI)
ACCUMULATE (64 MODULI)
BUFFER ADDRESSES & CONTROLS
242
A
B
246
LOG (A/B)
PEAK DETECT
AVERAGE PKS
250
CAPTURE TRACKING SAMPLES
FFT WINDOW TIMING & SYNC FSM
RESYNC
GUARD
IQGI
SINCGI
RX_GUARD
FFT_LOCK
SR_SWEEP
FFT WINDOW

FIG.23

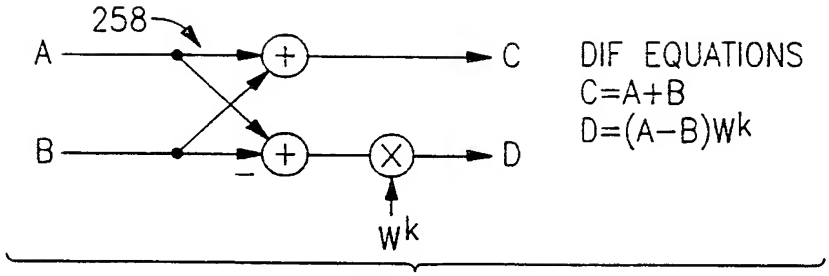


FIG.24

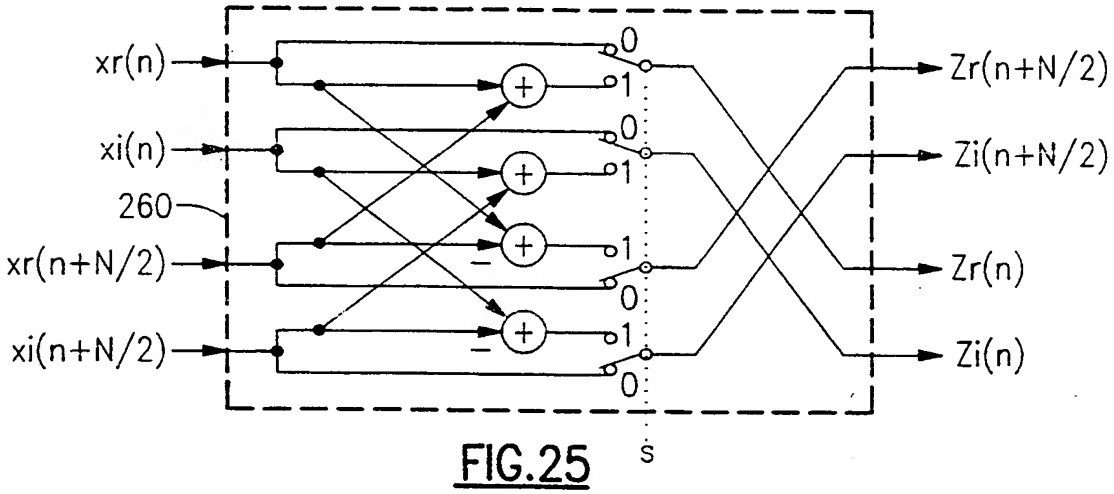


FIG.25
Prior Art

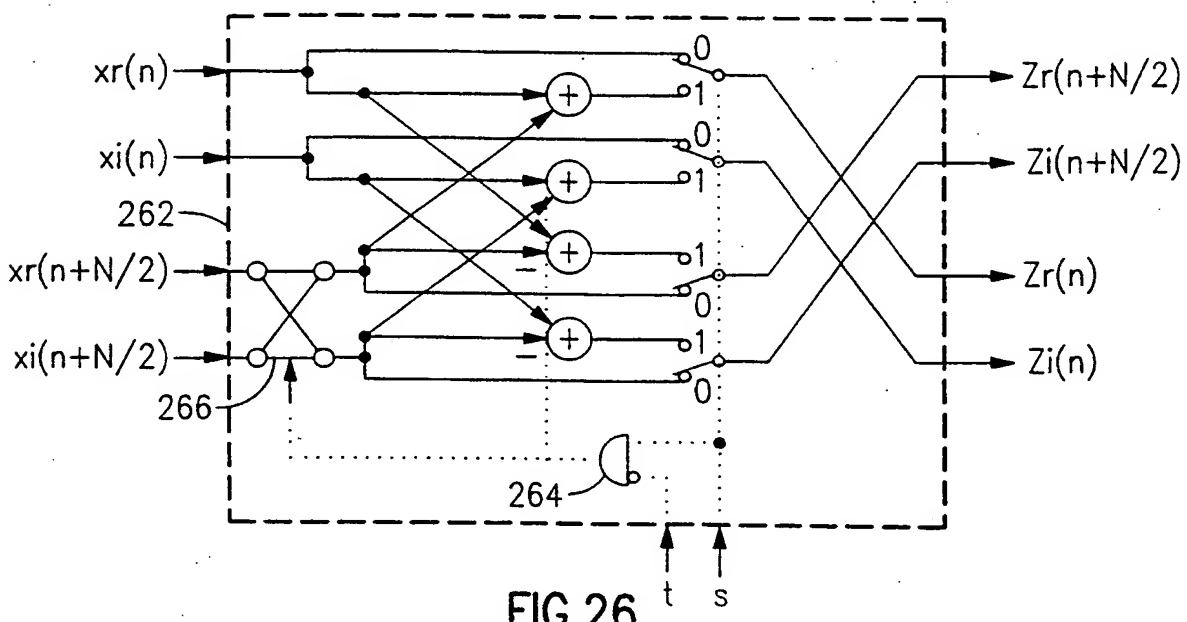
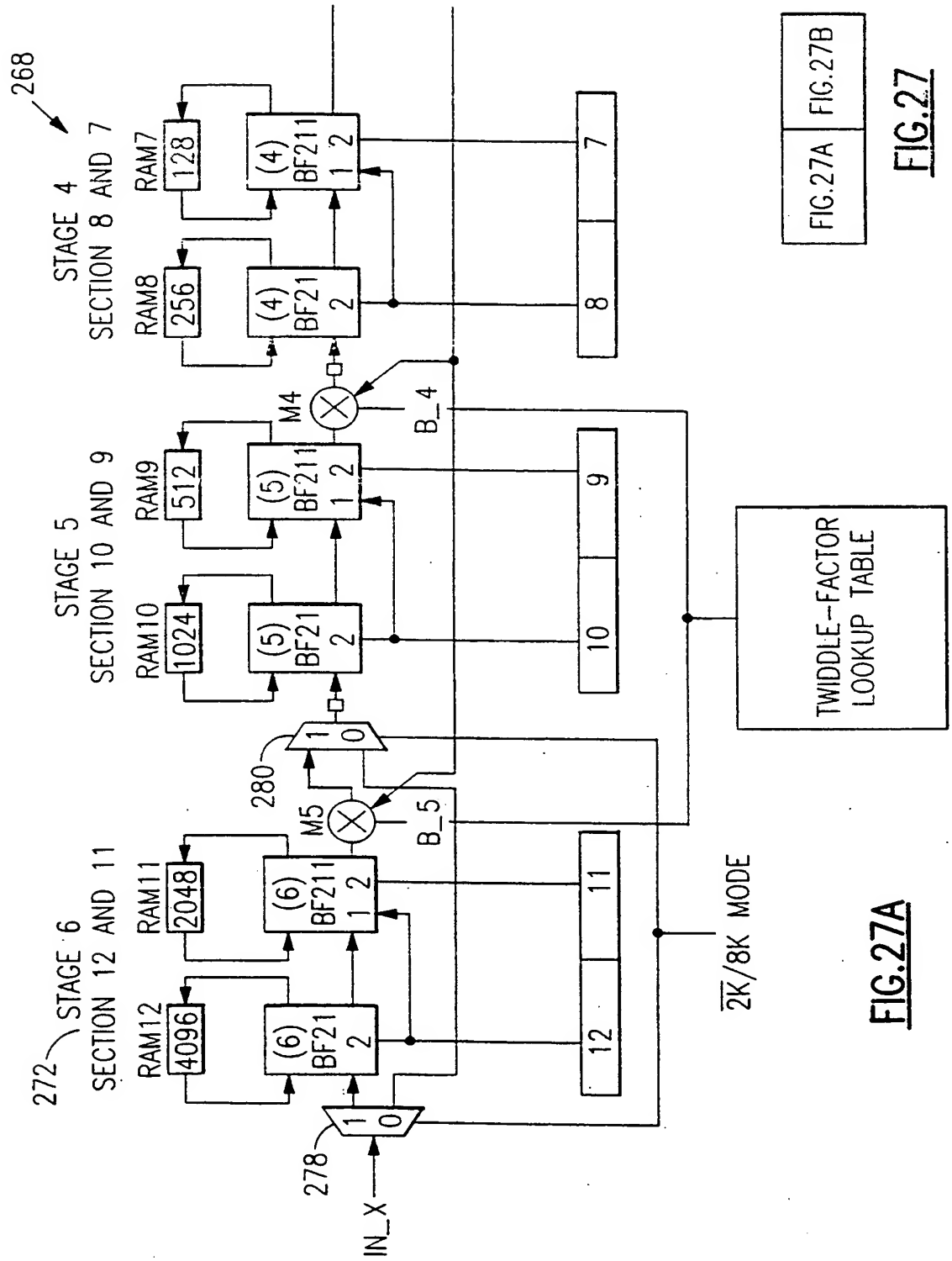


FIG.26
Prior Art



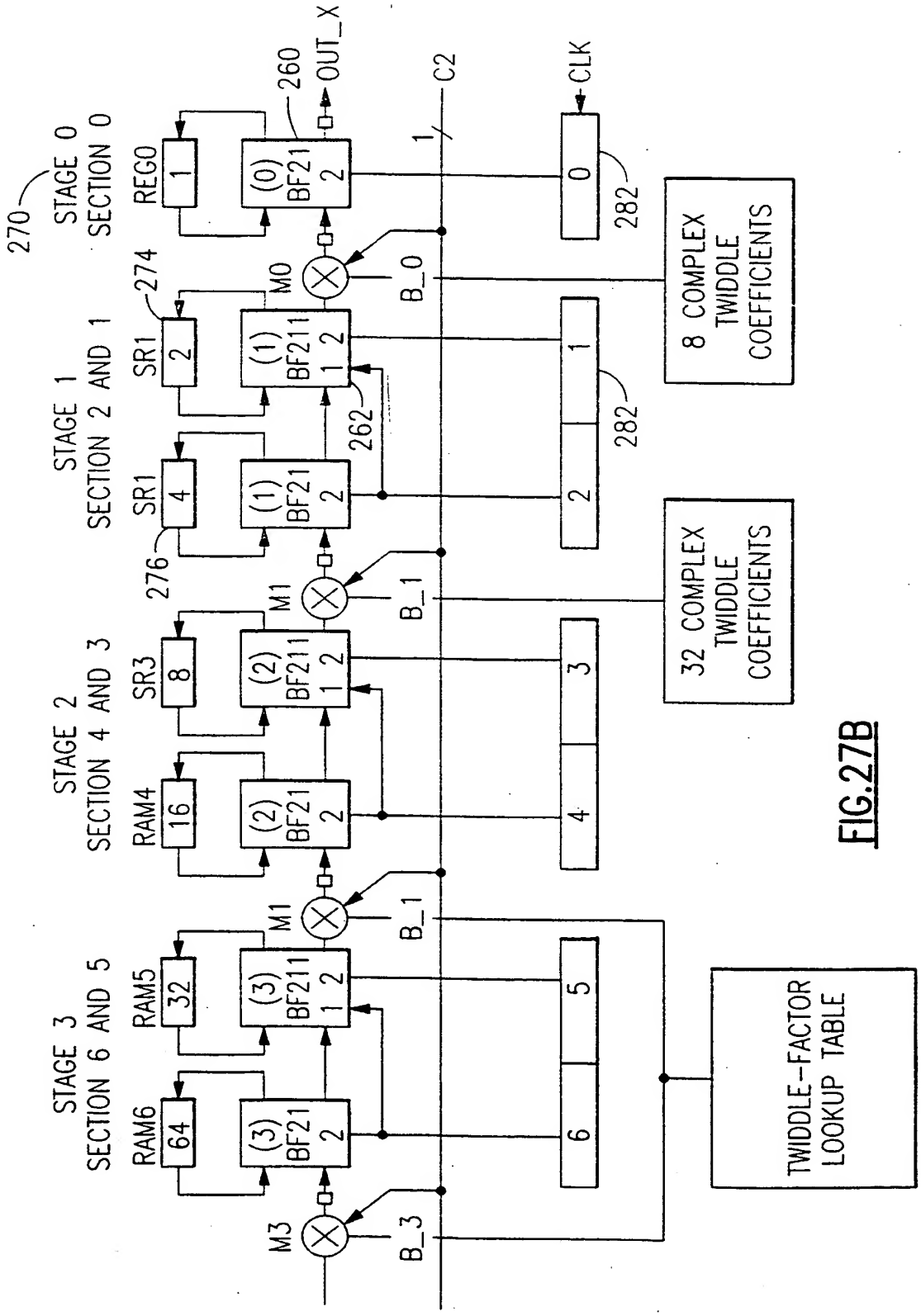


FIG.27B

FIG.28

FIG.28A	FIG.28B

FIG.28A

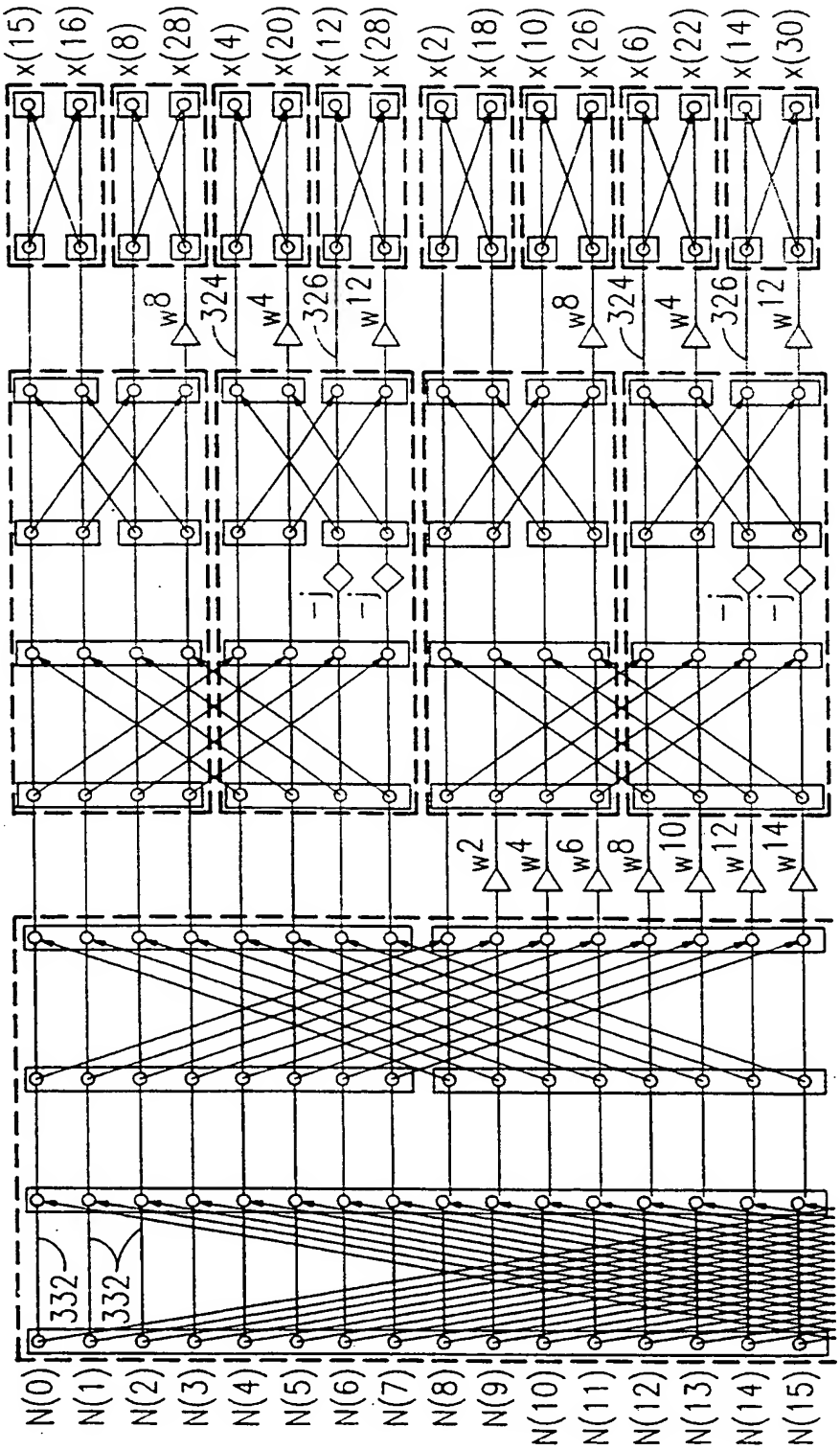
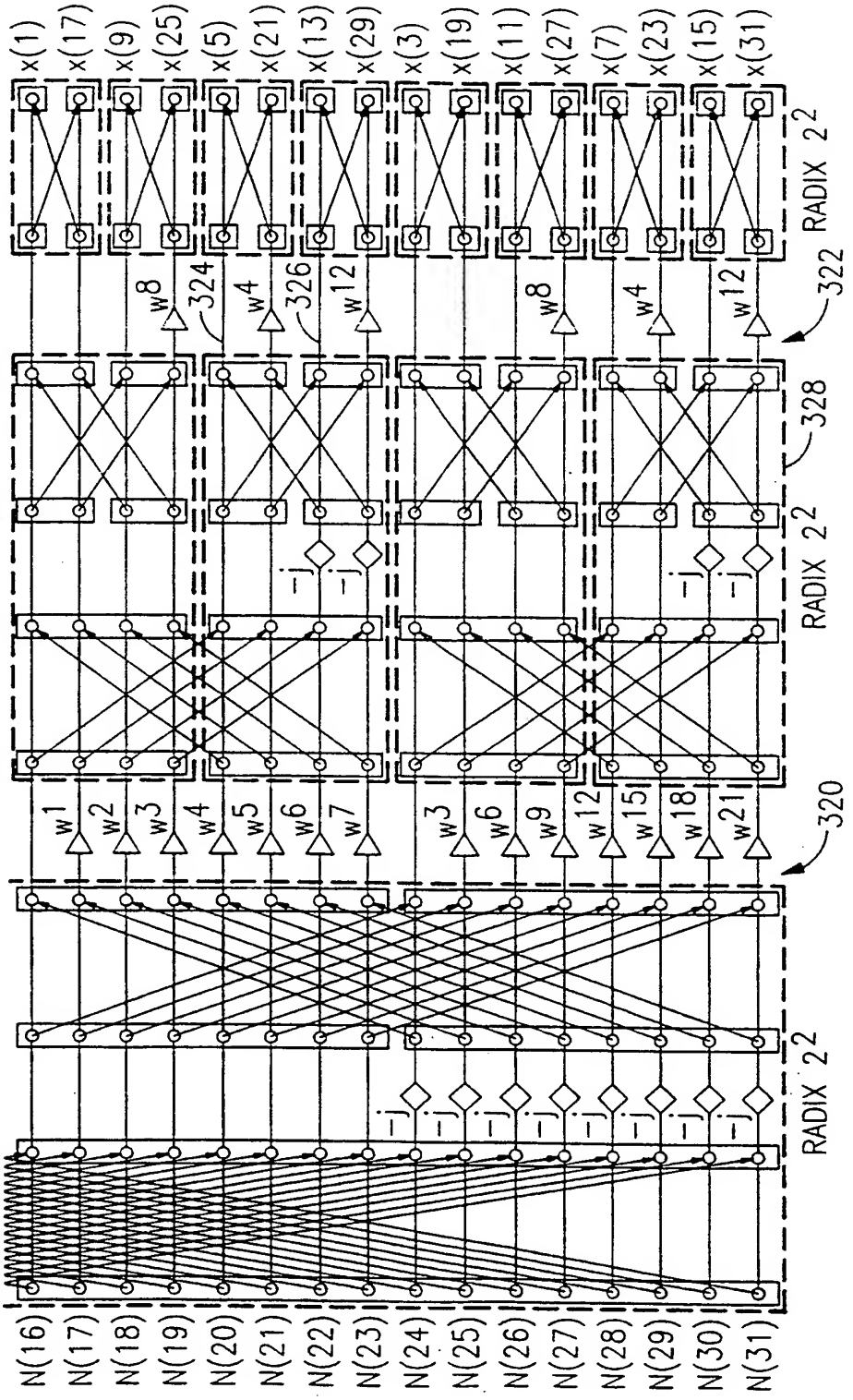


FIG.28B



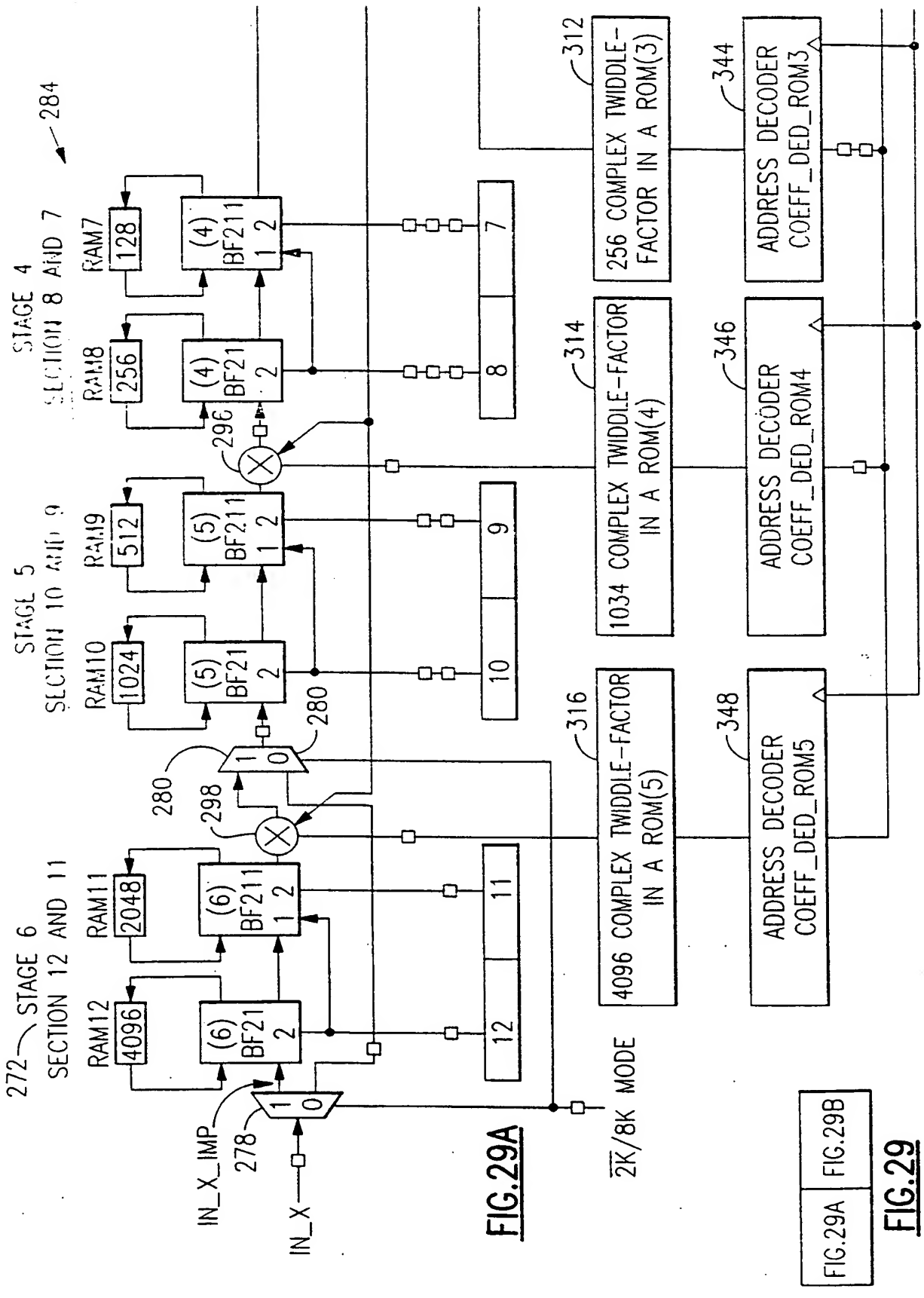


FIG.29A

FIG.29

FIG.29A | FIG.29B

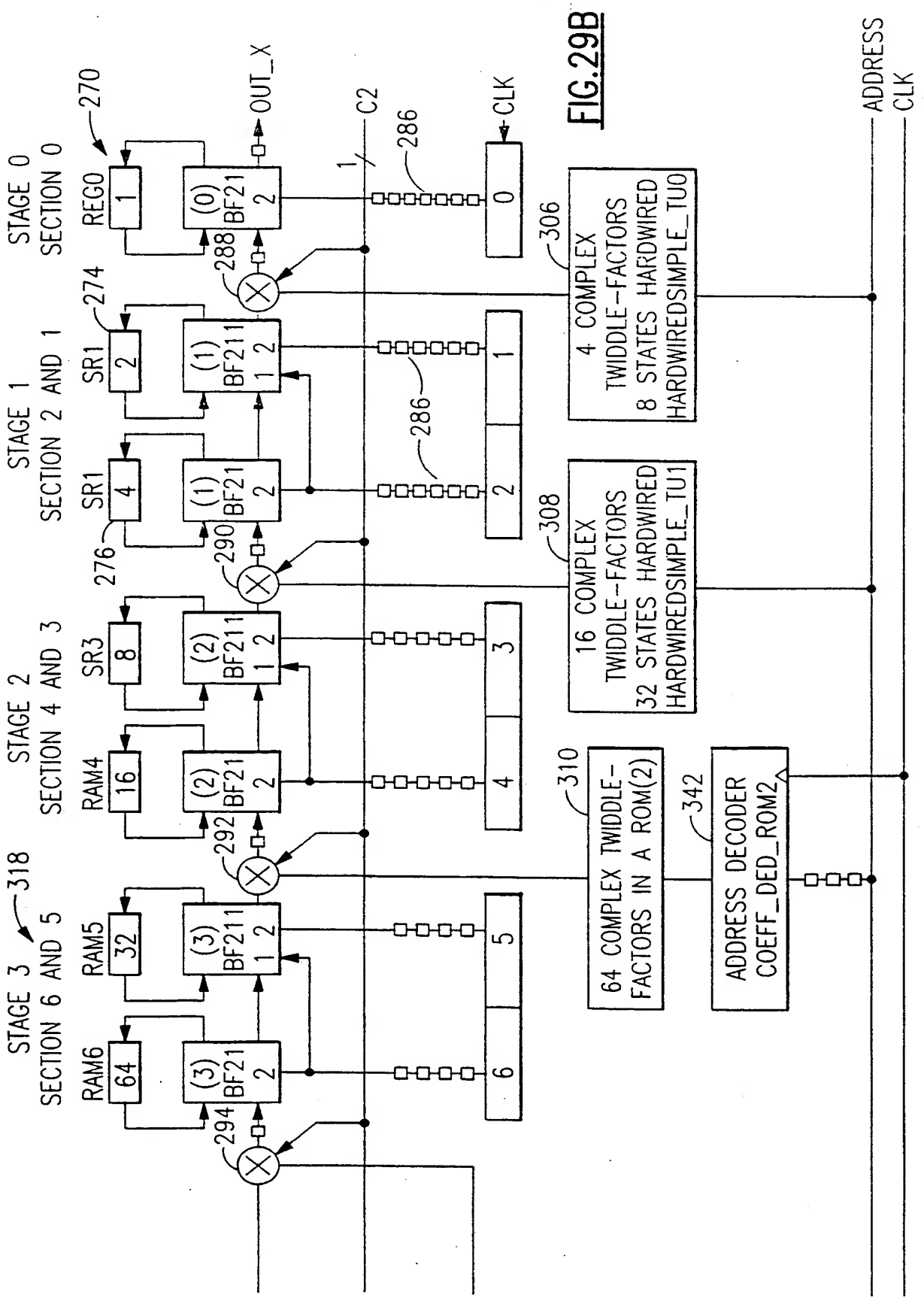


FIG.29B

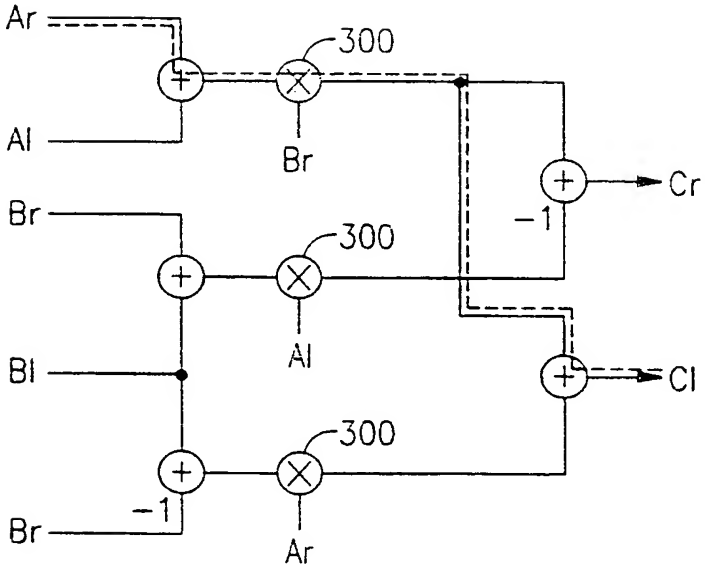

Ar
Al
300
Br
Cr
-1
Br
300
Al
Bl
Cl
300
-1
Br
Ar

FIG.30

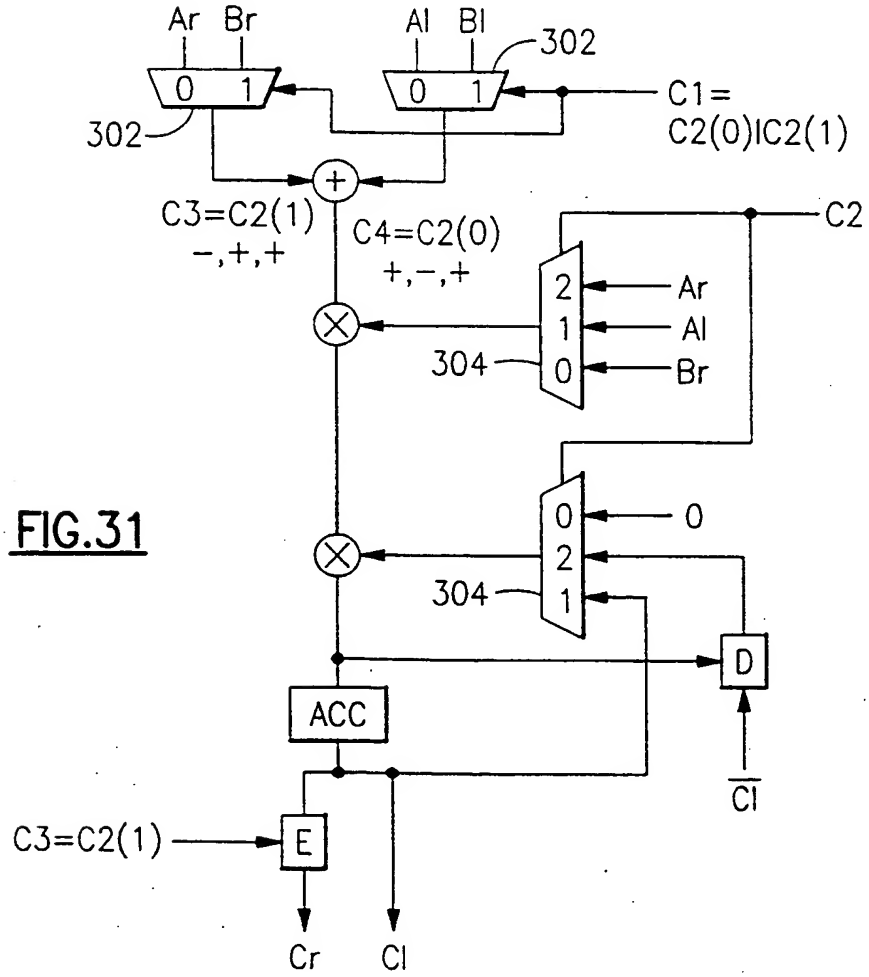

Ar Br
Al Bl
302
0 1
0 1
302
C1=
C2(0)IC2(1)
C3=C2(1)
-,+,+
C4=C2(0)
+,-,+
C2
2
1
0
Ar
Al
Br
304
0
2
1
0
304
D
ACC
C3=C2(1)
E
Cr
Cl
Cl

FIG.31

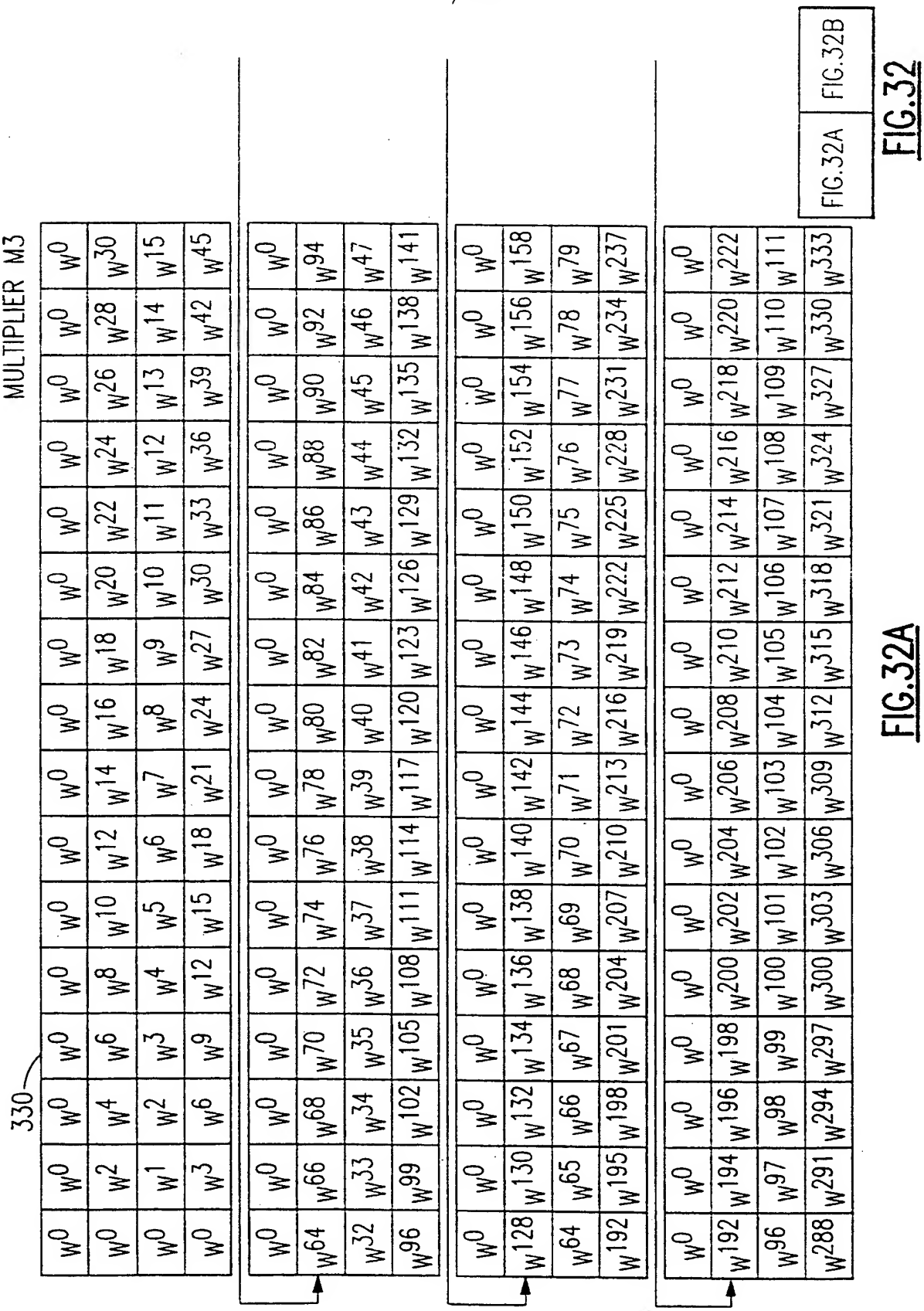


FIG.32B

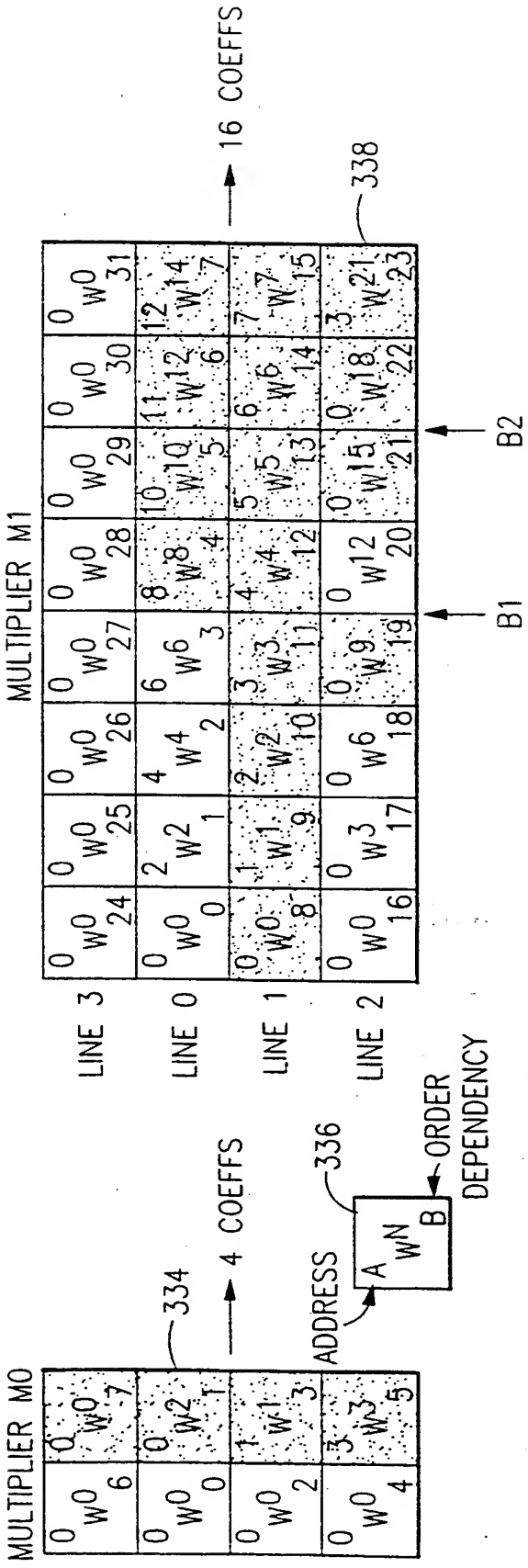


FIG.33A

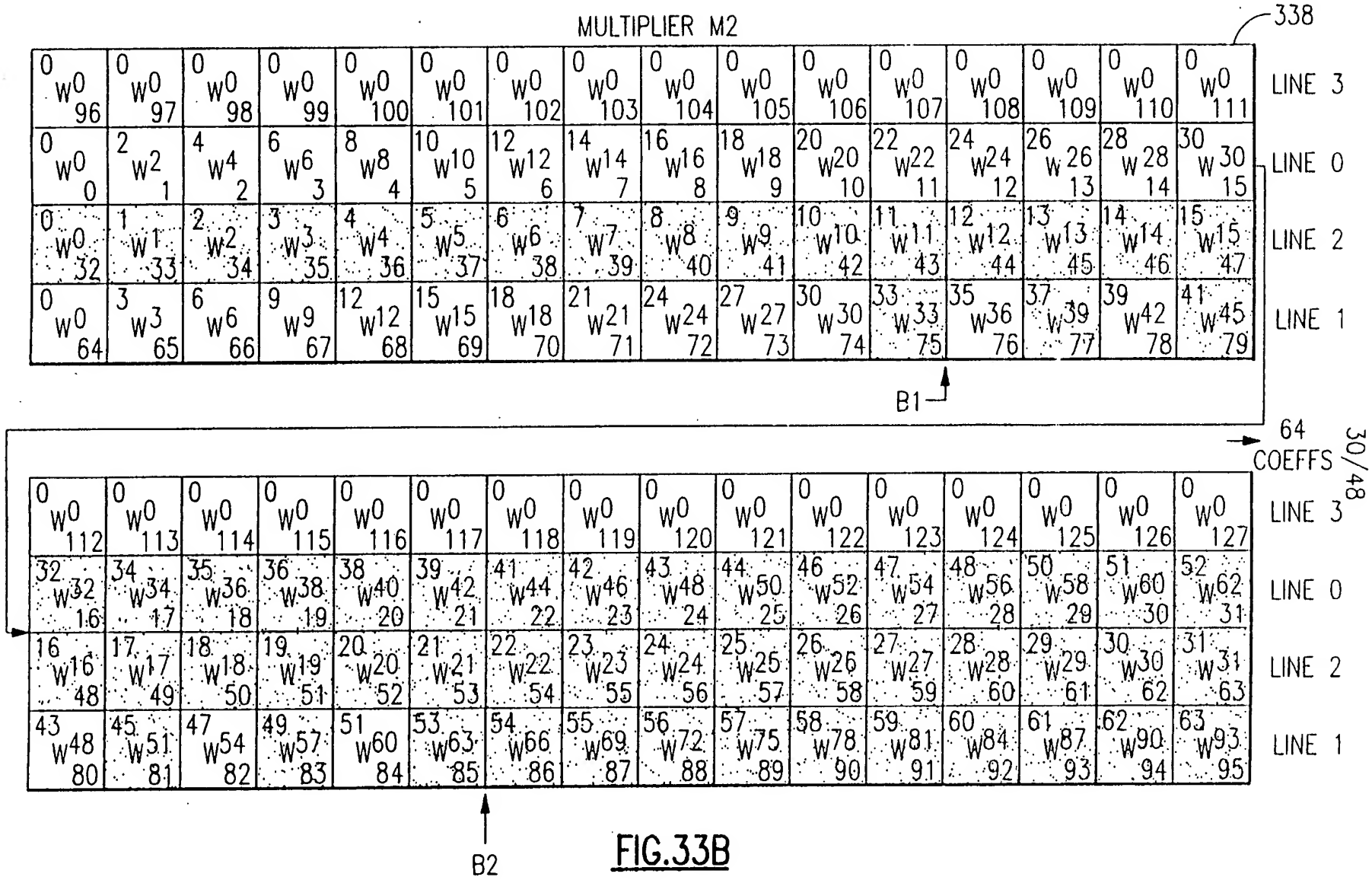


FIG.33B

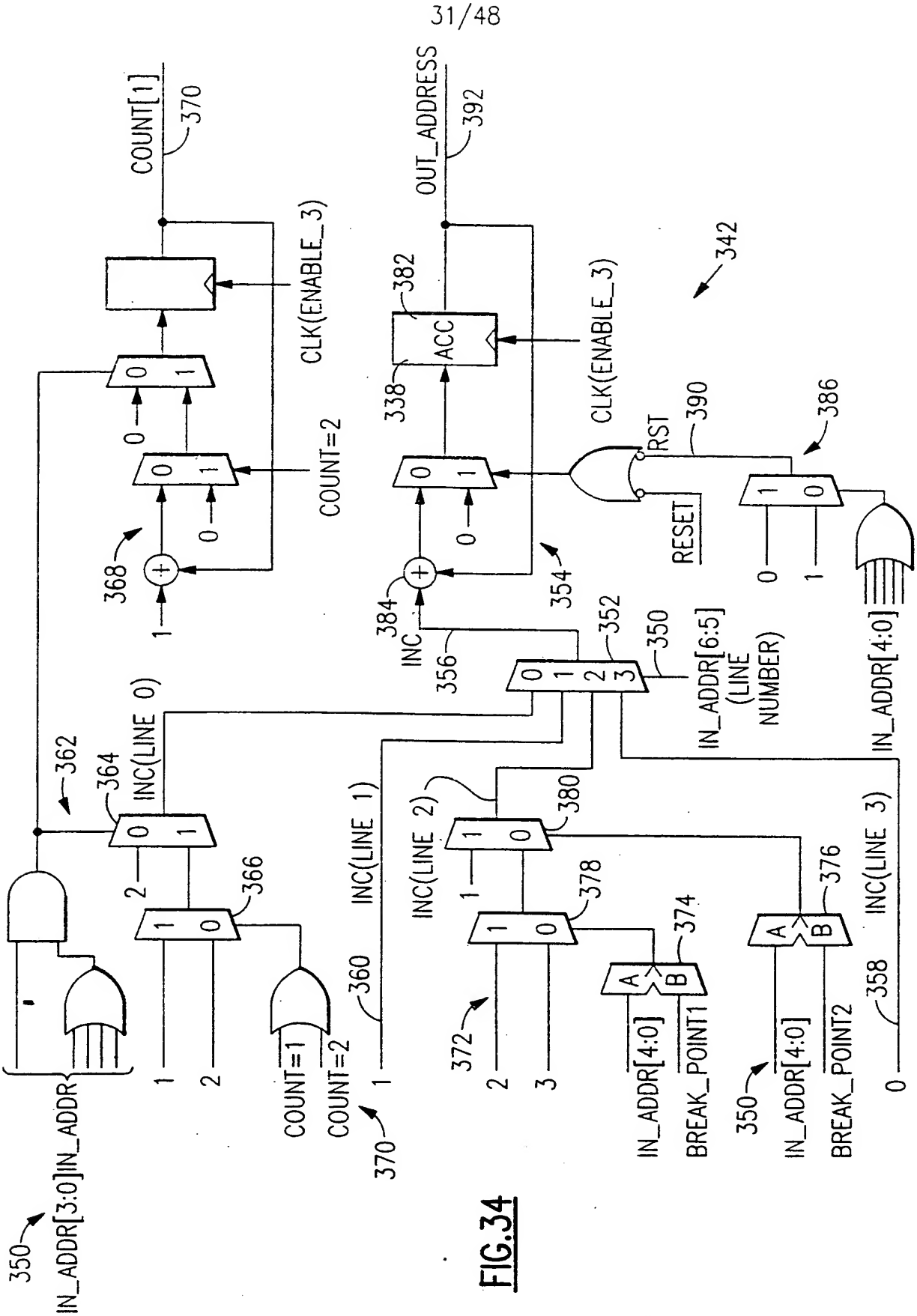


FIG.34

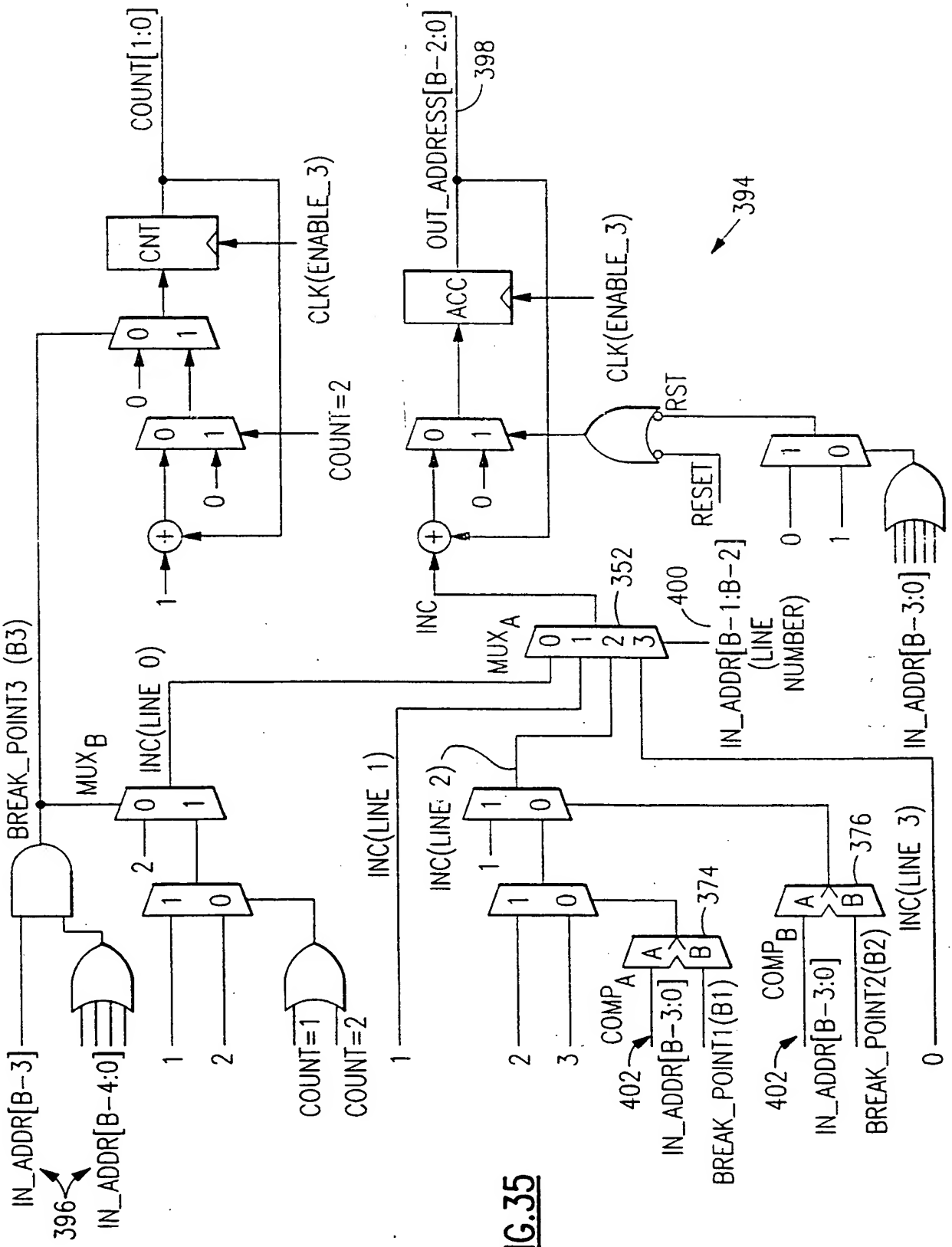


FIG.35

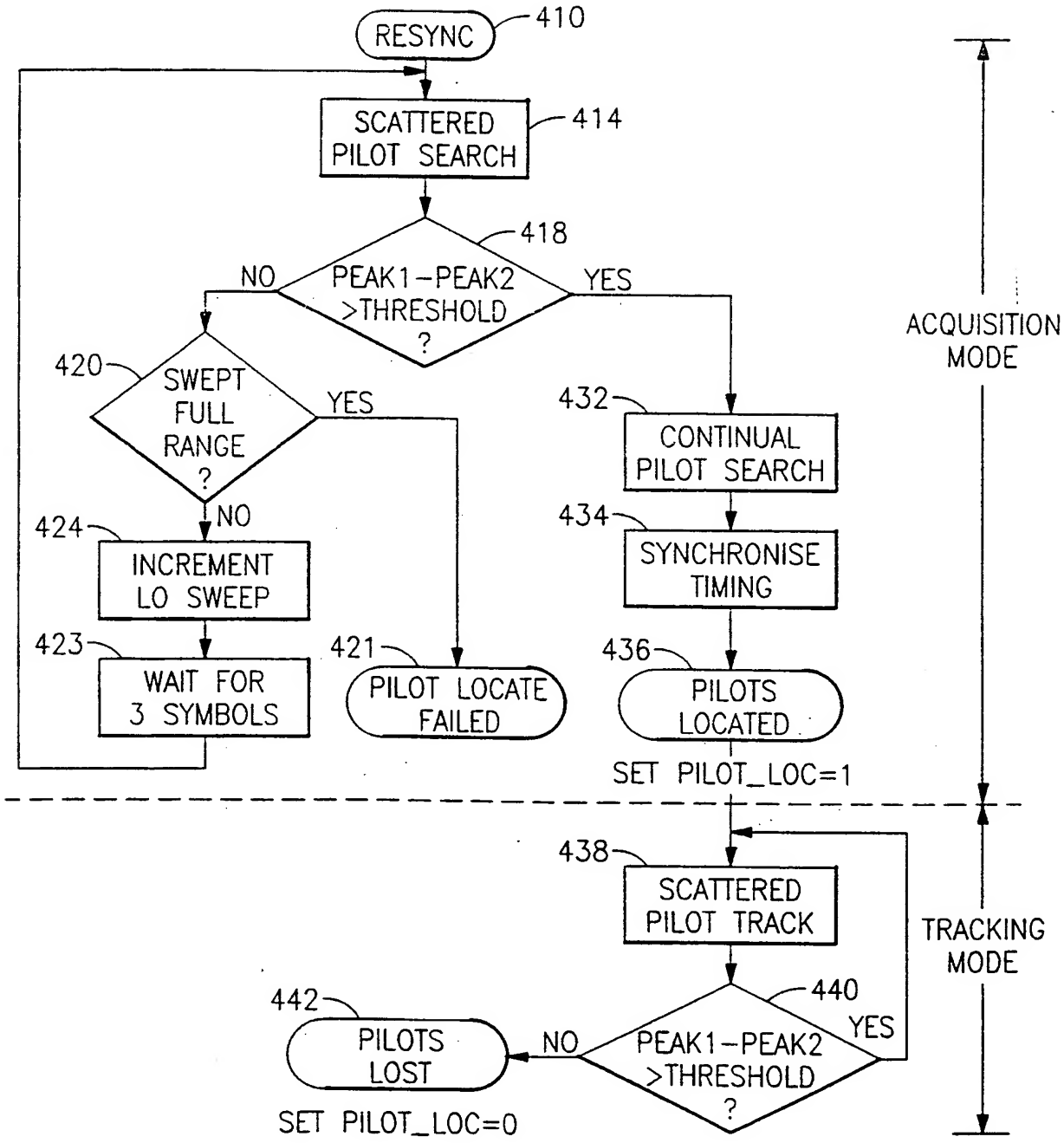


FIG.36

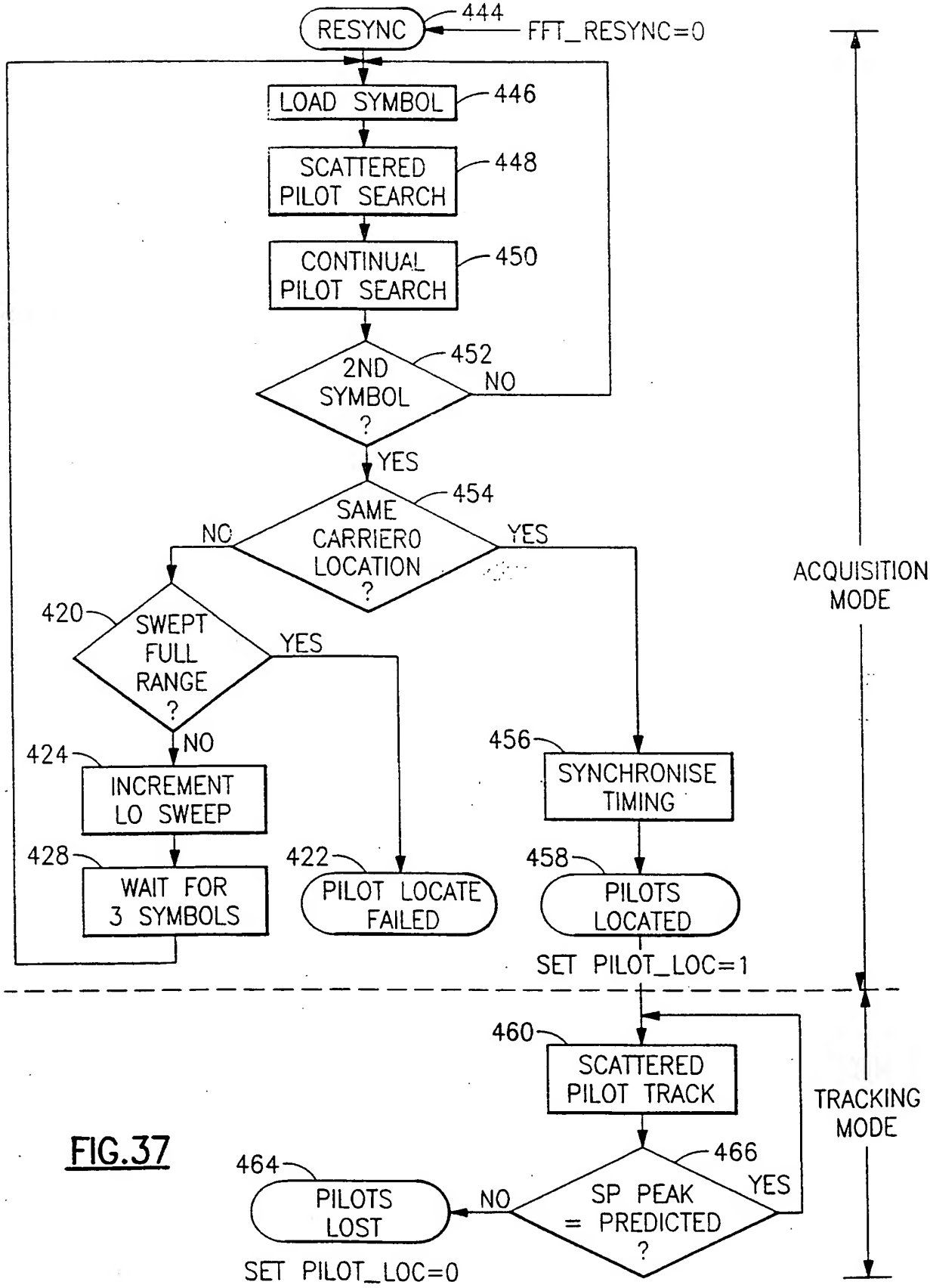


FIG.37

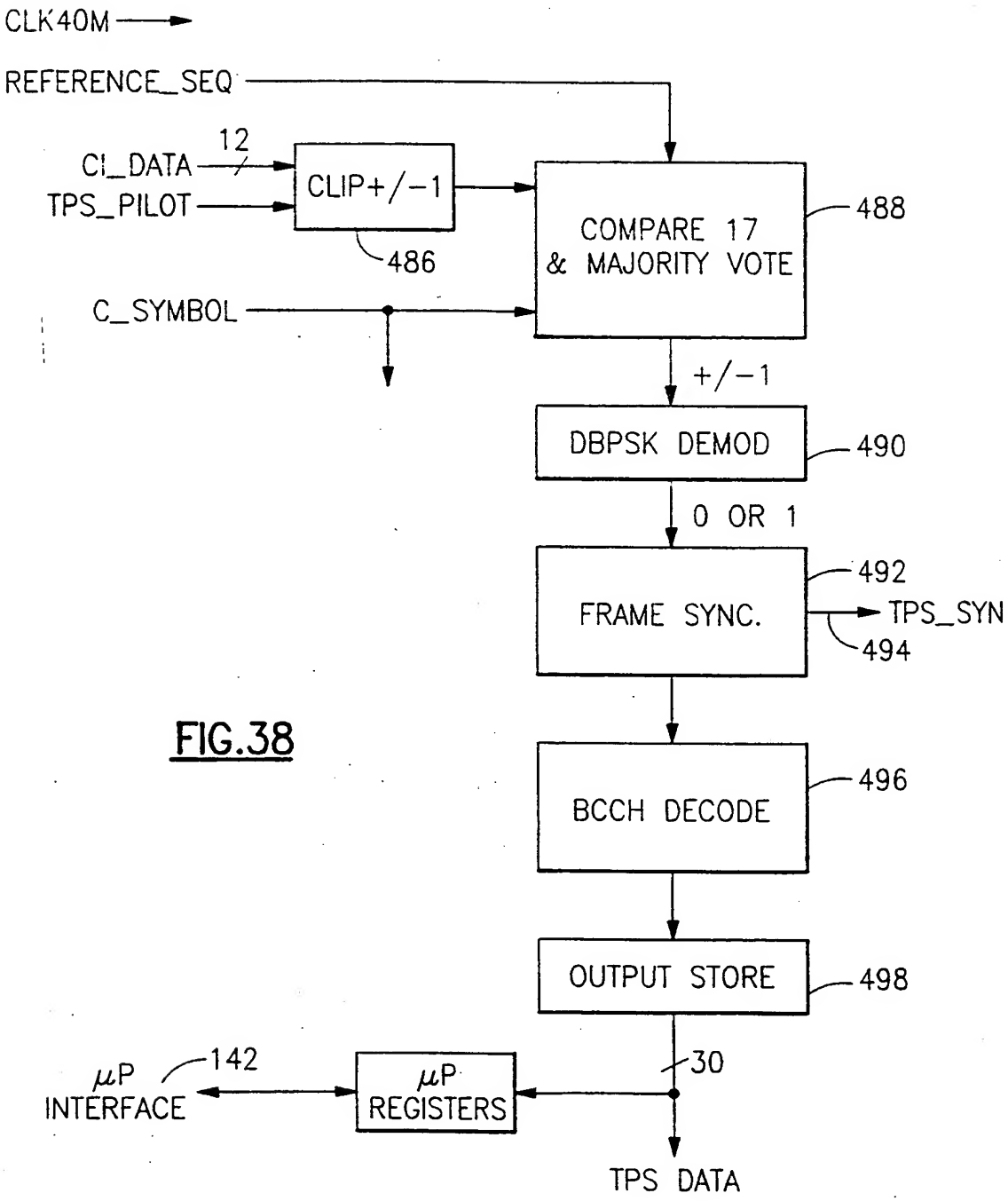


FIG.38

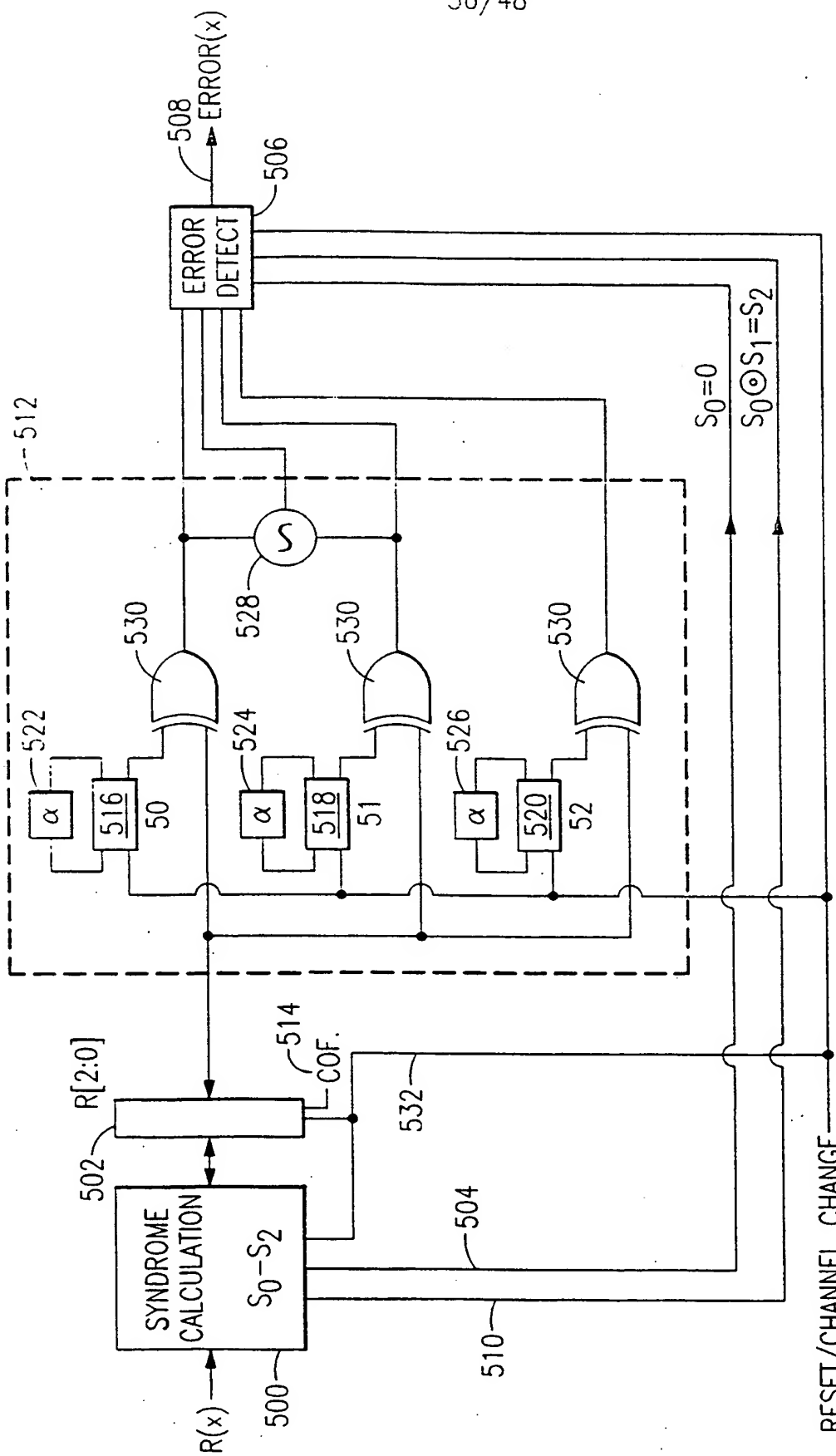

ERROR(x)
508
506
ERROR DETECT
512
$S_0=0$
$S_0 \odot S_1=S_2$
528
530
530
530
522
524
526
α
516
50
α
518
51
α
520
52
514
COF.
R[2:0]
502
532
SYNDROME CALCULATION
S_0-S_2
504
510
500
R(x)
RESET/CHANNEL CHANGE

FIG.39

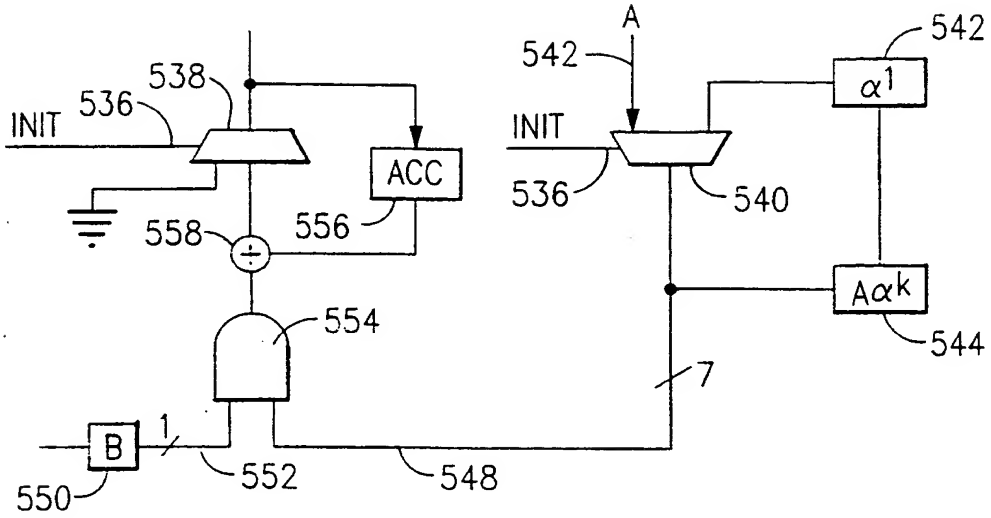


FIG.40

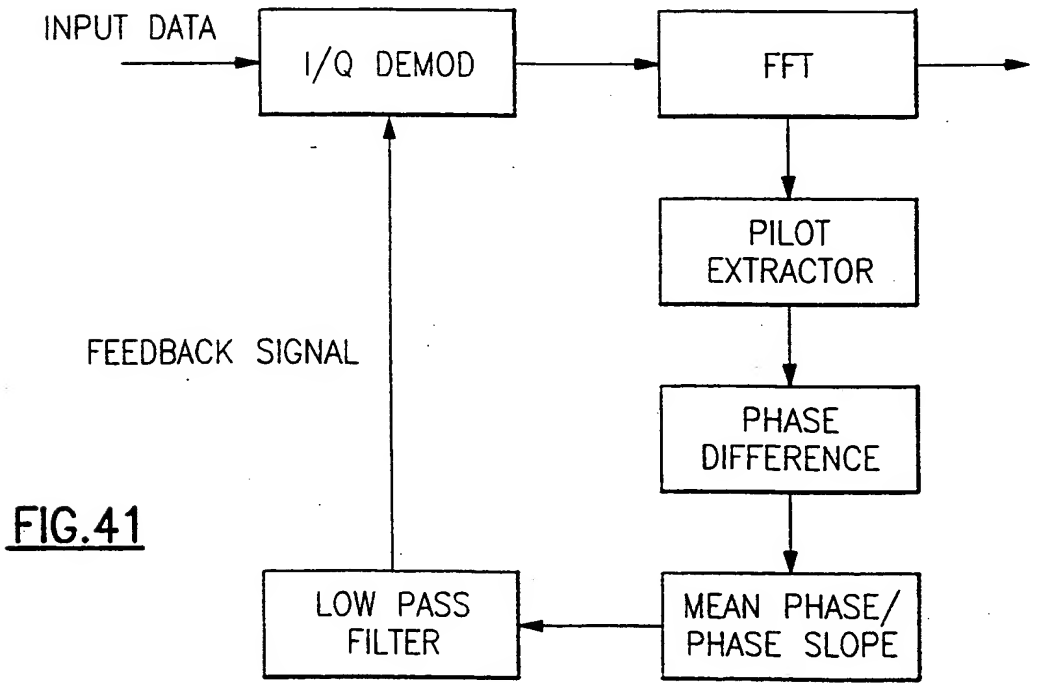
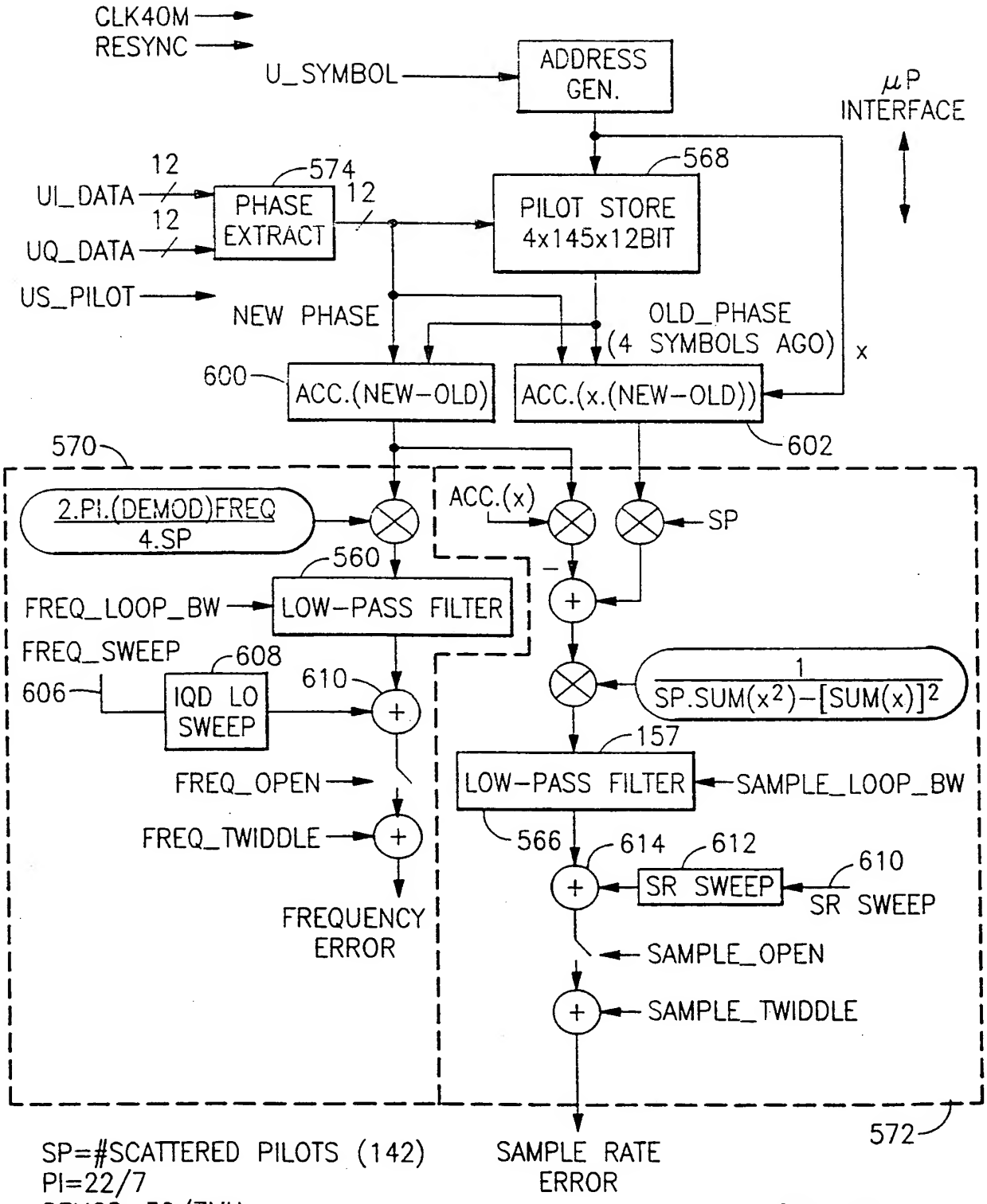


FIG.41



SP=#SCATTERED PILOTS (142)
PI=22/7
DEMOD=32/7MHz
ACC.=ACCUMULATION OF SP SAMPLES

FIG.42

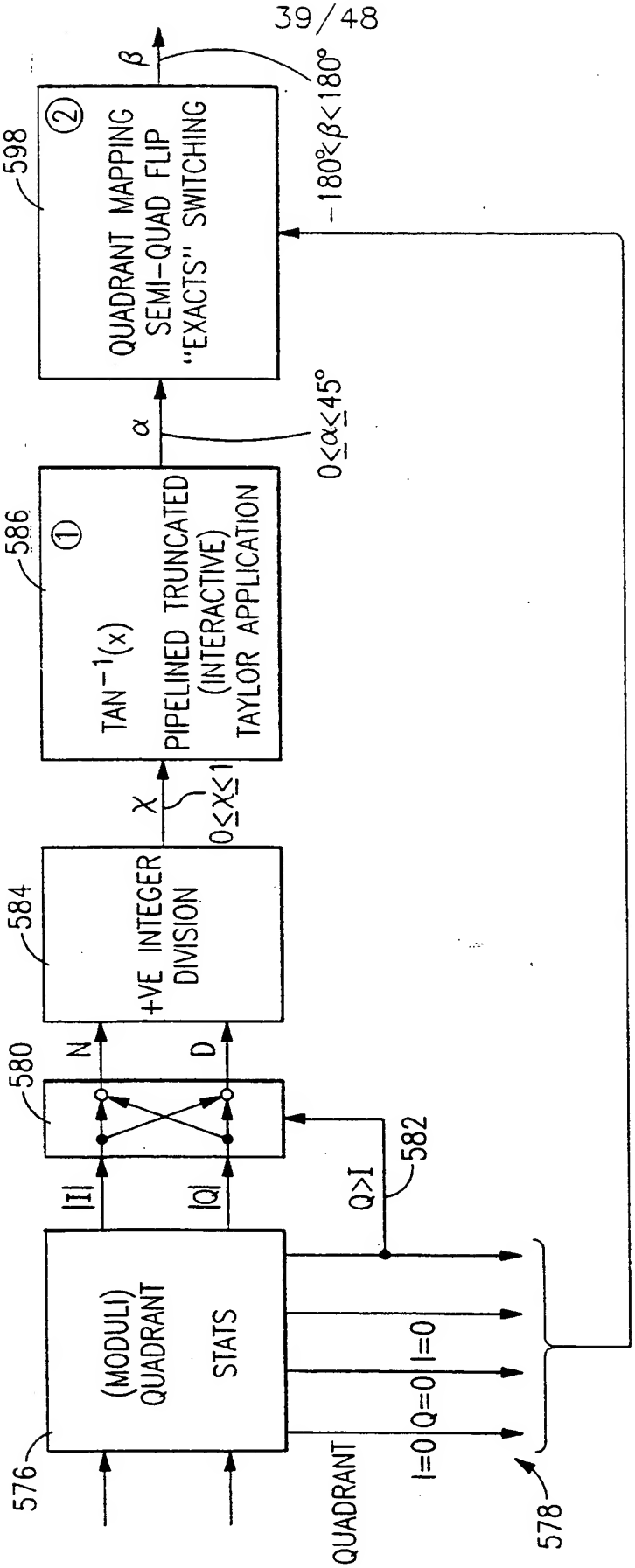


FIG.43

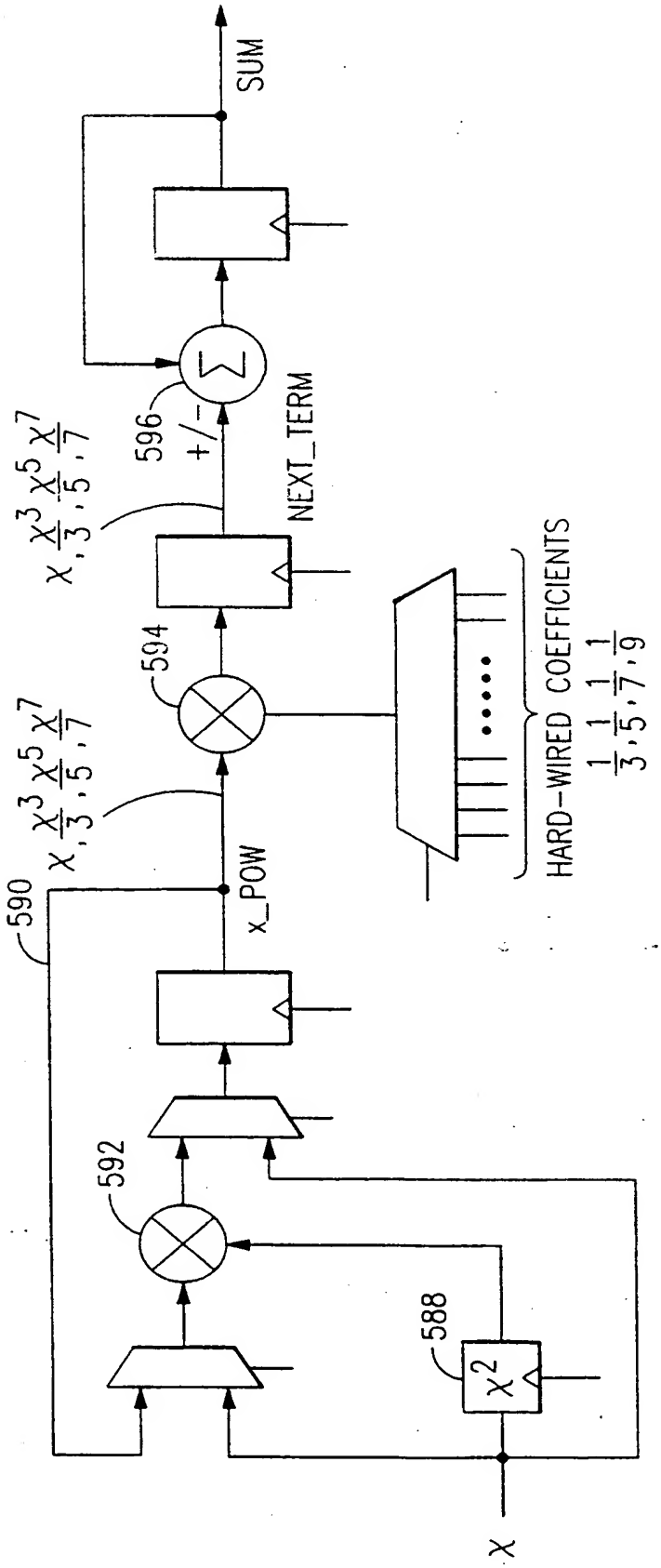


FIG.44

FIG.45

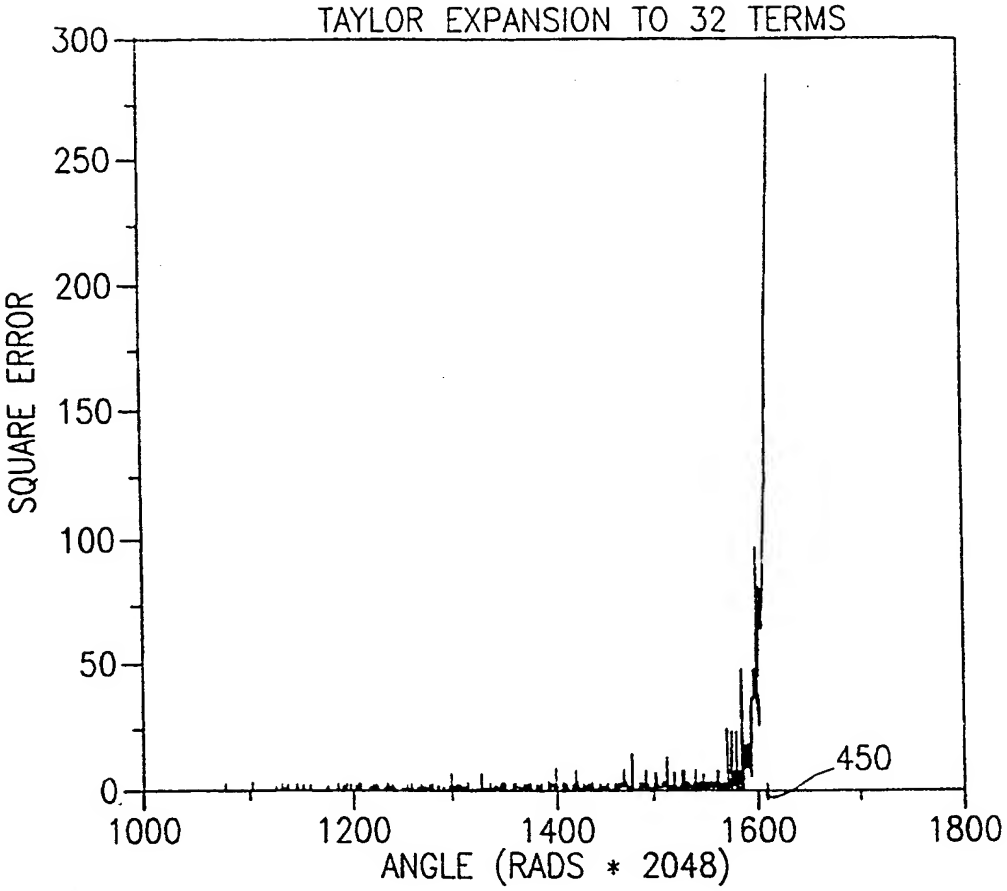


FIG.46

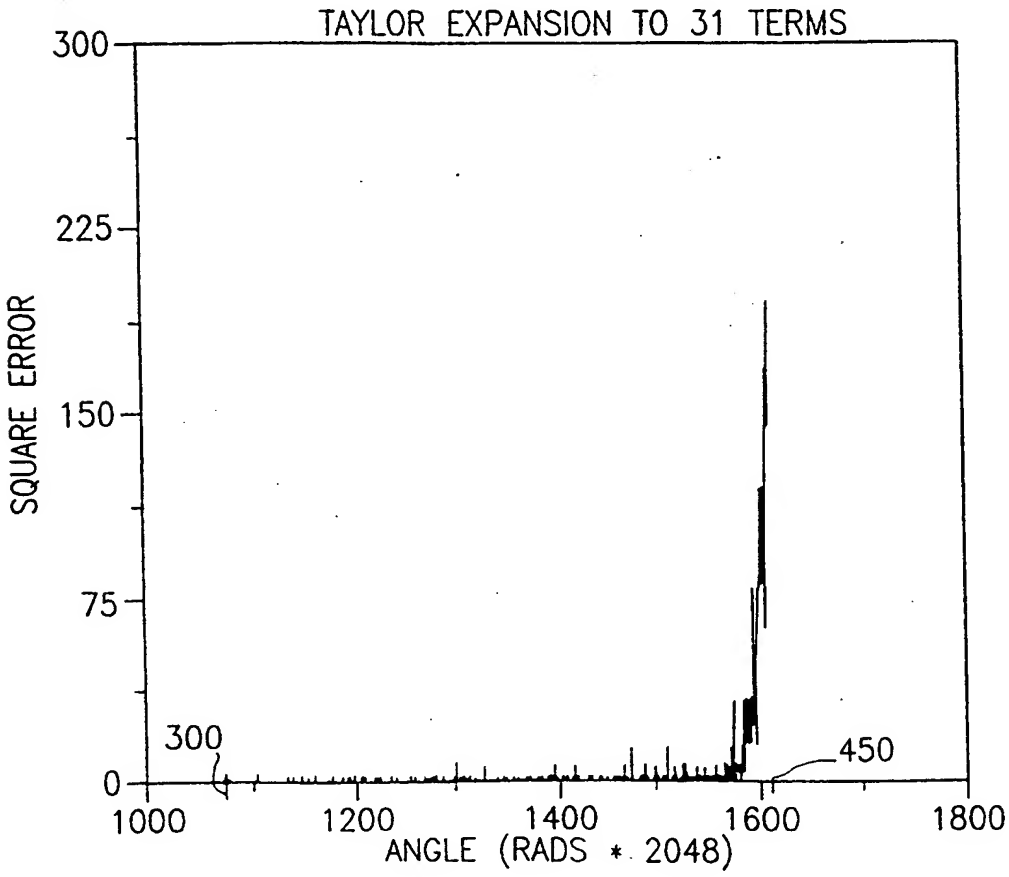
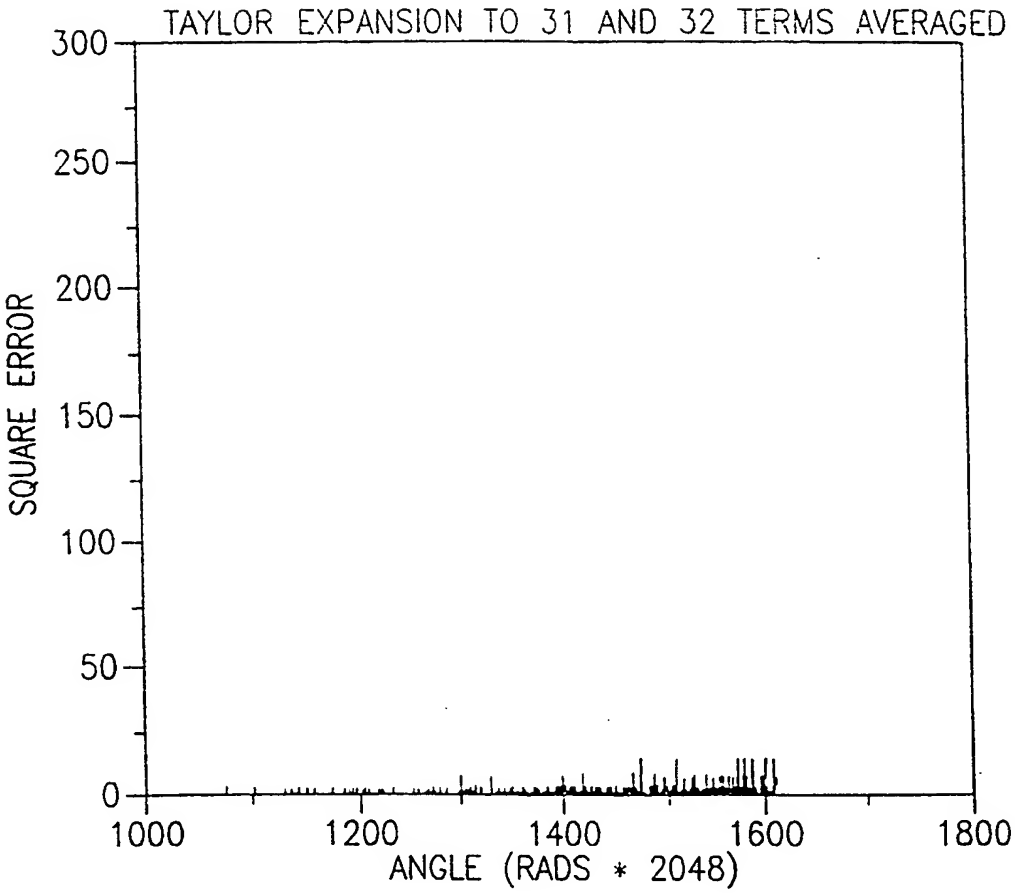


FIG.47



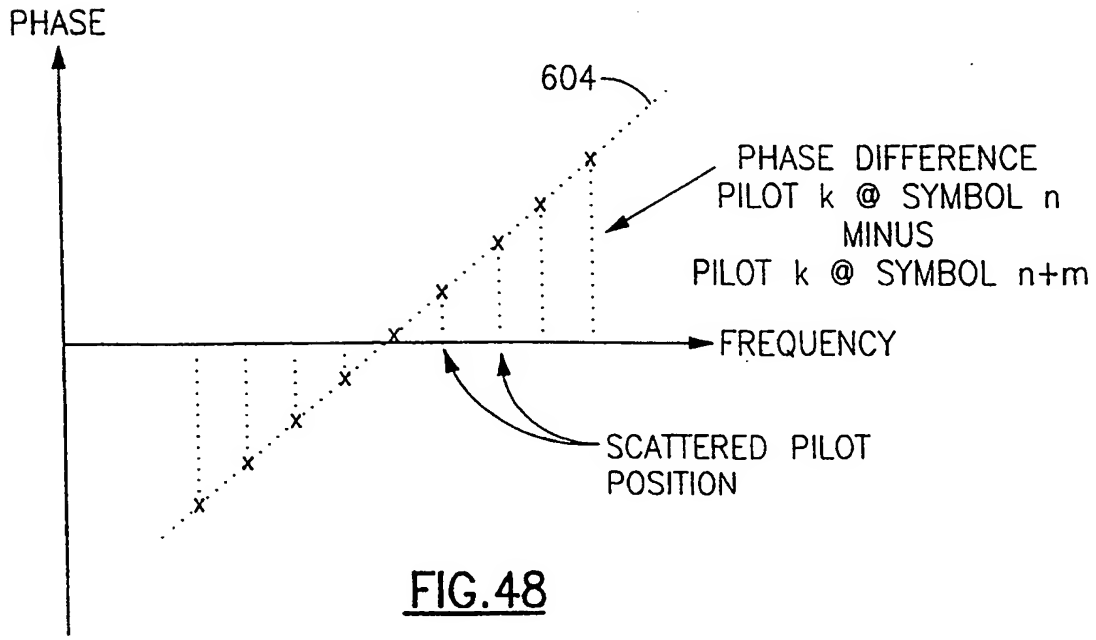
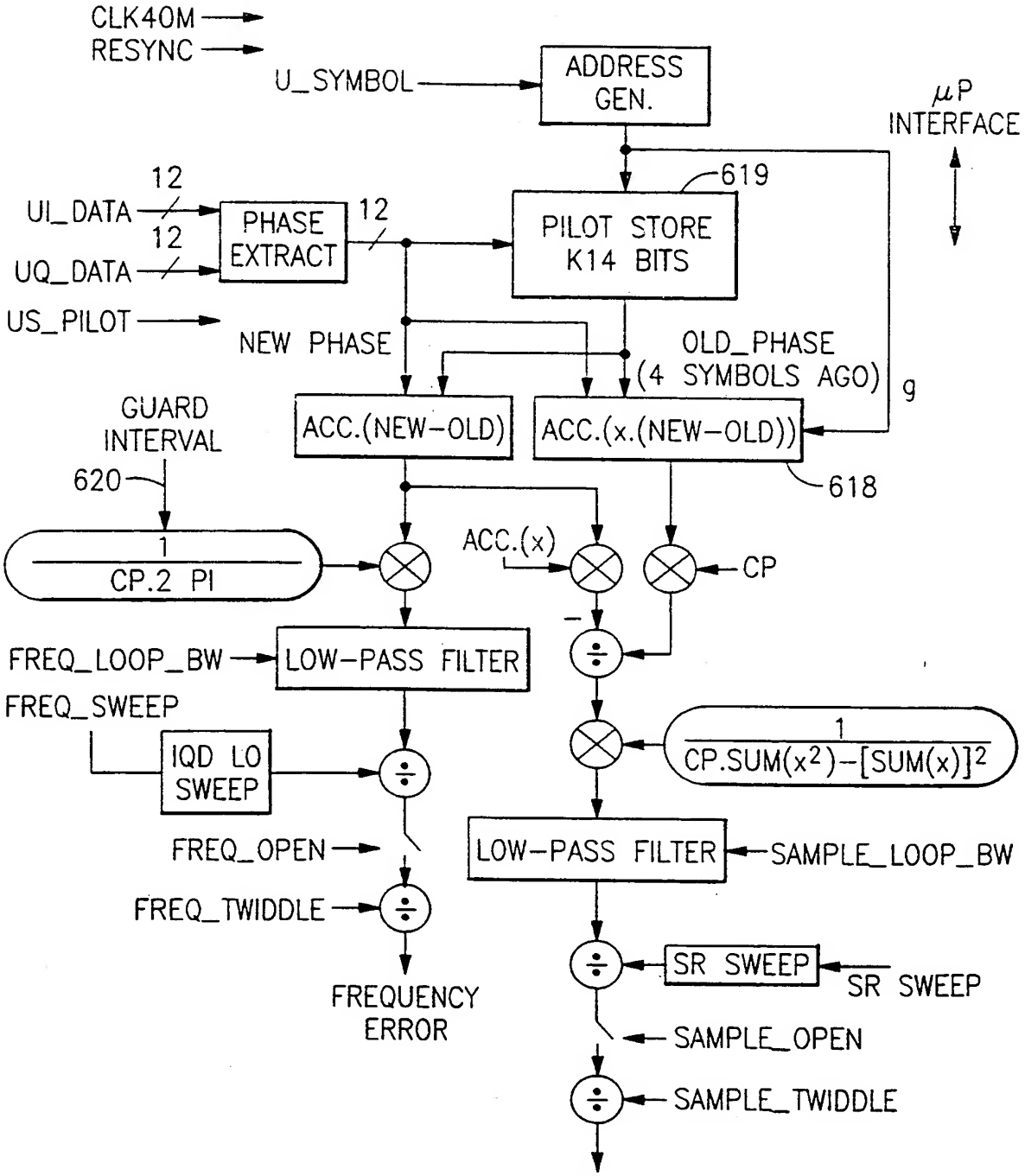


FIG.48



CP=#SCATTERED PILOTS (45)
PI=22/7
ACC.=ACCUMULATION OF SP SAMPLES
Tt=SYMBOL PERIOD (DEPENDS ON GUARD)
m=4(SYMBOLS BEFORE SP "PHASE" REPEATS)

FIG.49

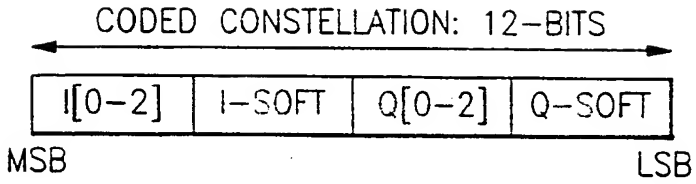


FIG.50

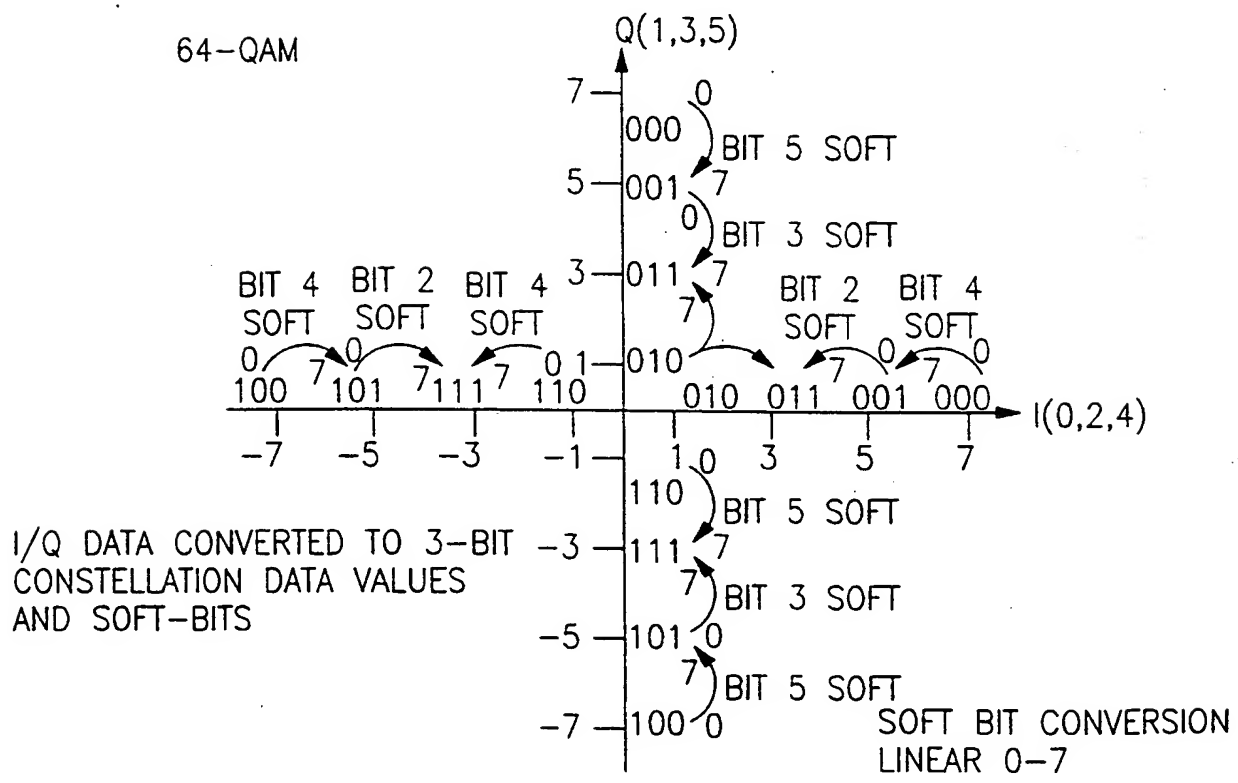


FIG.51

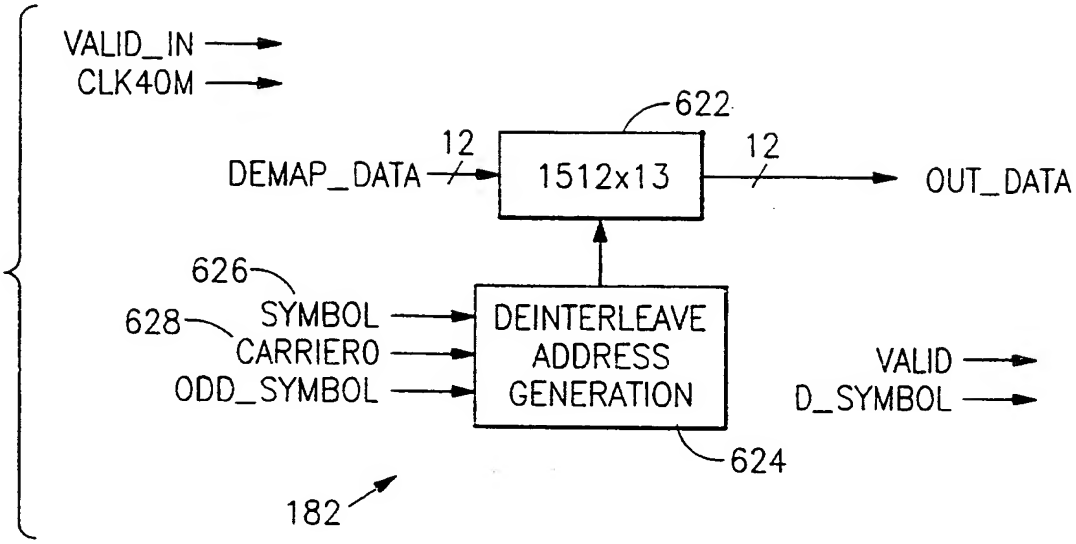


FIG.52

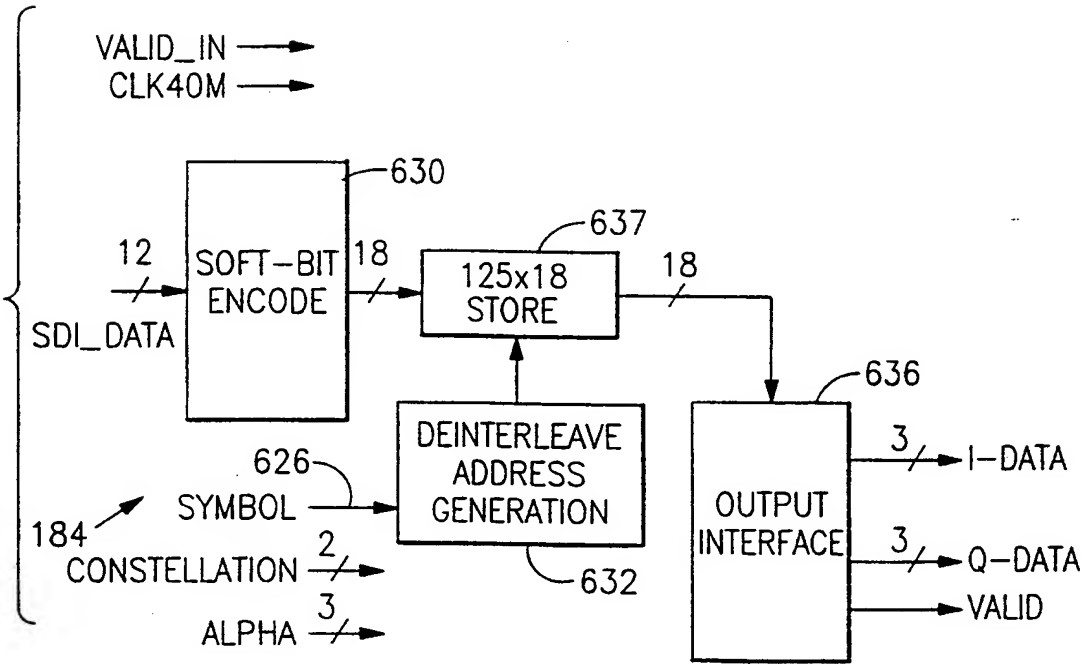


FIG.53

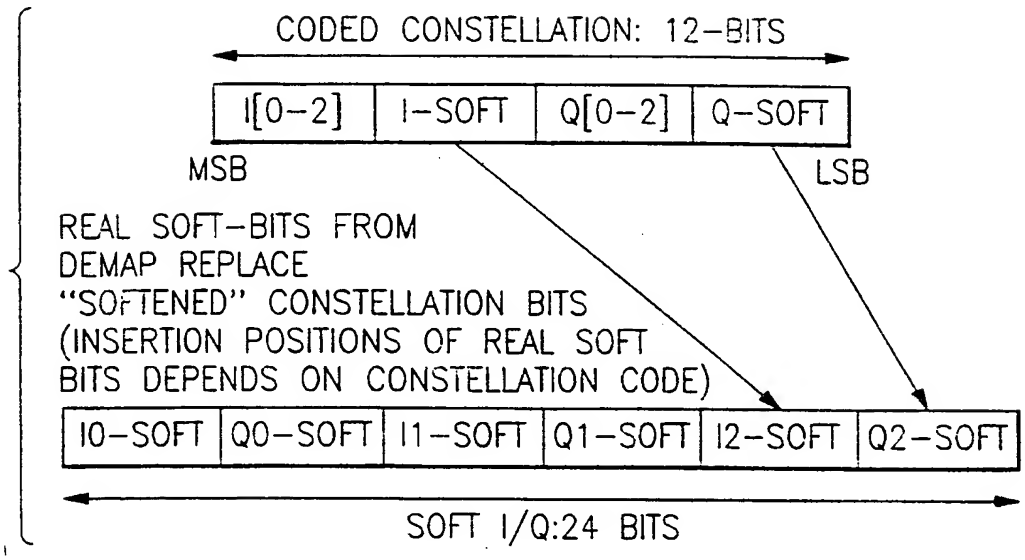


FIG.54

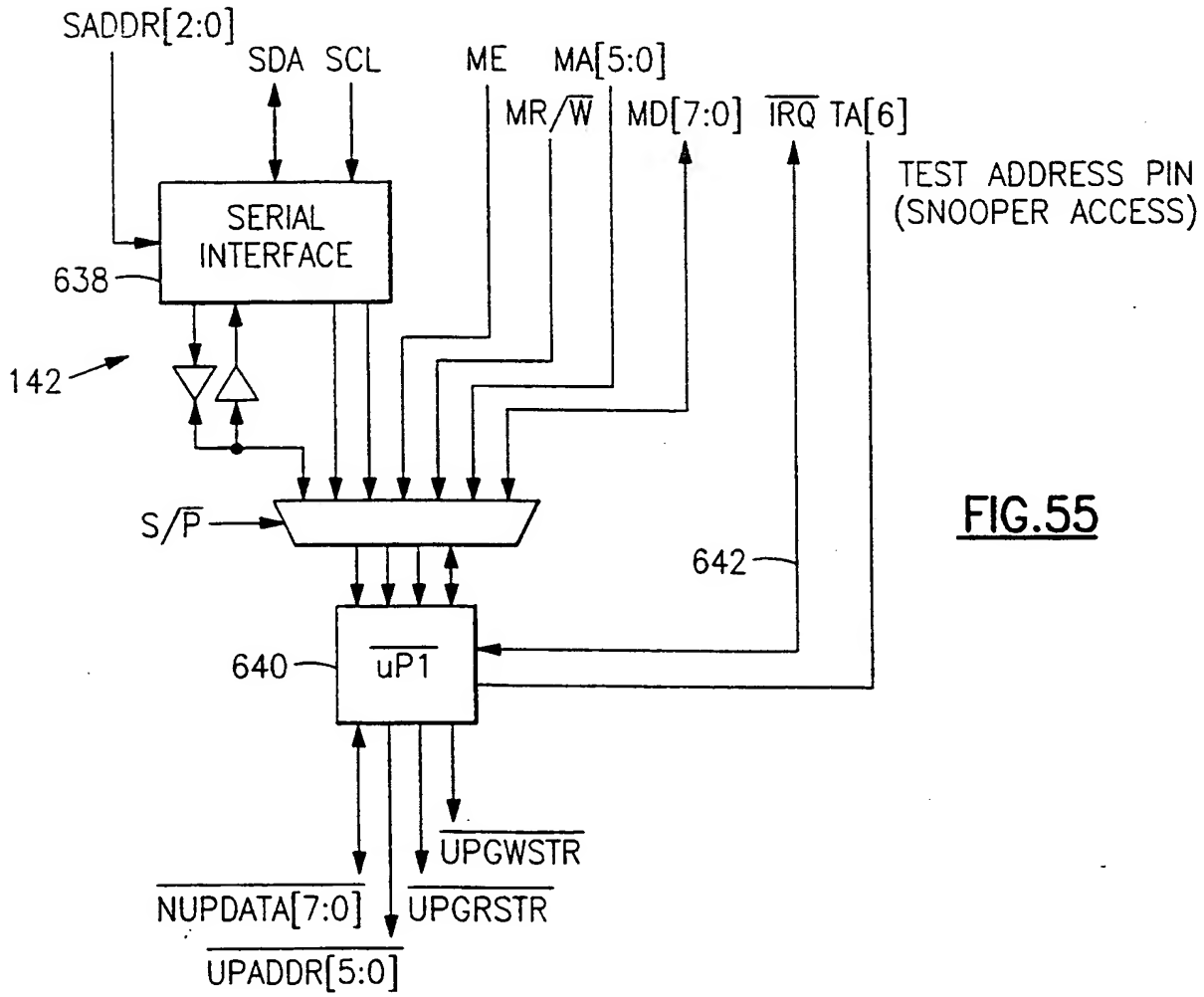


FIG.55

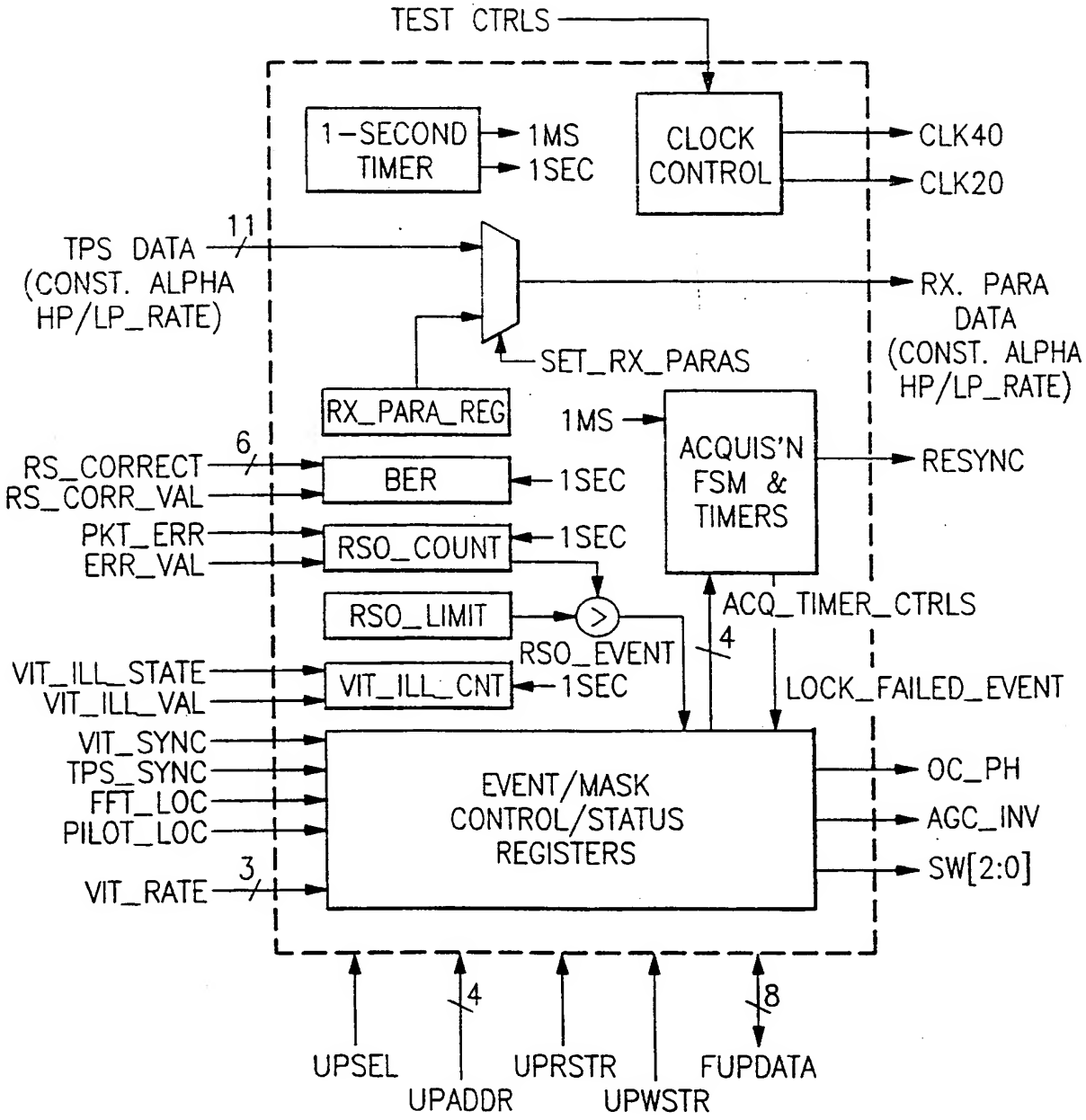


FIG.56

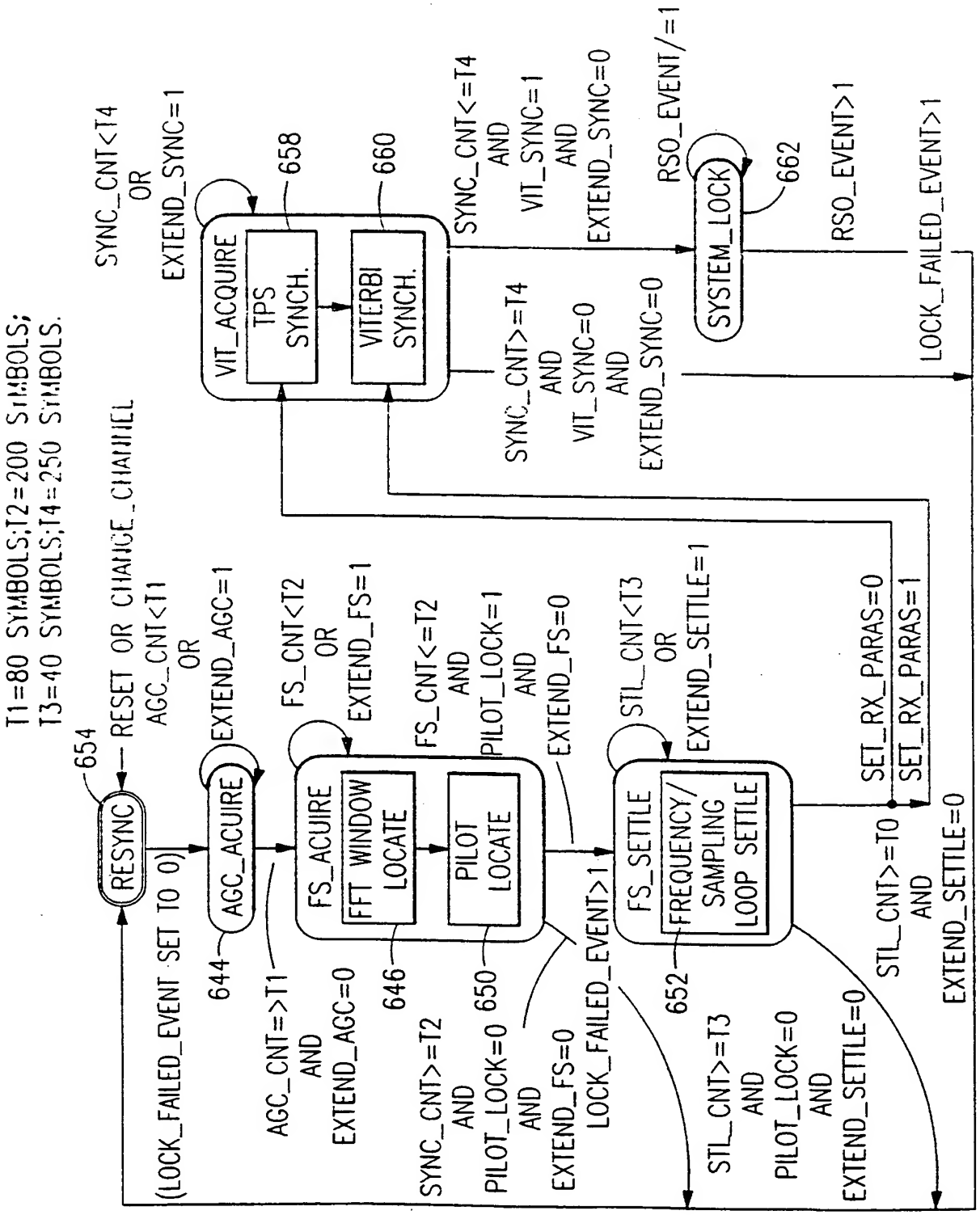


FIG.57

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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H04L 27/26, G06F 17/14, H04L 1/00 A3

(11) International Publication Number: **WO 98/19410**

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9720550.4	26 September 1997 (26.09.97)	GB

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(74) Agent: BICKEL, Arthur, S.; Suite 200, 2355 Main Street, P.O. Box 19616, Irvine, CA 92623 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
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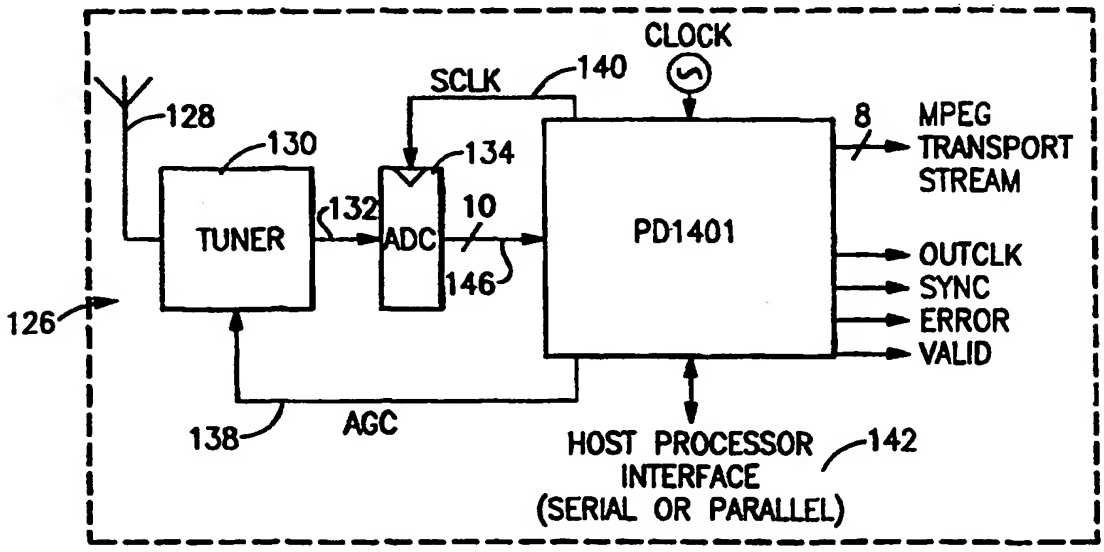
27 August 1998 (27.08.98)

(54) Title: SINGLE CHIP VLSI IMPLEMENTATION OF A DIGITAL RECEIVER EMPLOYING ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING



(57) Abstract

The invention provides a single chip implementation of a digital receiver for multicarrier signals that are transmitted by orthogonal frequency division multiplexing. Improved channel estimation and correction circuitry are provided. The receiver has highly accurate sampling rate control and frequecy control circuitry. BCH decoding of tps data carriers is achieved with minimal resources with an arrangement that includes a small Galois field multiplier. An improved FFT window synchronization circuit is coupled to the resampling circuit for locating the boundary of the guard interval transmitted with the active frame of the signal. A real–time pipelined FFT processor is operationally associated with the FFT window synchronization circuit and operates with reduced memory requirements.

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INTERNATIONAL SEARCH REPORT

Inter. nal Application No
PCT/US 97/18911

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L27/26 G06F17/14 H04L1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 730 357 A (TELIA AB) 4 September 1996 see abstract see figure 1 see figure 10	1,4
A		2

Y	US 4 300 229 A (HIROSAKI BOTARO) 10 November 1981 see abstract see column 15, line 15 - line 32; figure 4 see column 39, line 59 - line 60	1,4
A		

A	EP 0 653 858 A (TOKYO SHIBAURA ELECTRIC CO) 17 May 1995 see abstract see figure 5	1,2

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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2

Date of the actual completion of the international search	Date of mailing of the international search report
5 March 1998	07. 07. 98

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Koukourlis, S

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WIRELESS PERSONAL COMMUNICATIONS, vol. 2, no. 4, 1 January 1996, pages 321-334, XP000589621 WYATT-MILLINGTON W ET AL: "A PIPELINED IMPLEMENTATION OF THE WINOGRAD FFT FOR SATELLITE ON-BOARD MULTI-CARRIER DEMODULATION" see page 321, paragraph 2 - paragraph 3 ---	1
A	WO 95 03656 A (TELIA AB ;ISAKSSON MIKAEL (SE); ENGSTROEM BO (SE)) 2 February 1995 see abstract see page 7, line 15 - line 20 see figure 4 ---	1
A	WO 96 24989 A (ADC TELECOMMUNICATIONS INC) 15 August 1996 see page 61, line 26 - page 62, line 6 see page 84, line 4 - page 85, line 9 see figures 11,27 ---	1
A	EP 0 722 235 A (MATSUSHITA ELECTRIC IND CO LTD) 17 July 1996 see figure 2 ---	1
A	EP 0 689 314 A (NOKIA TECHNOLOGY GMBH) 27 December 1995 see figure 2 -----	1

2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 97/ 18911

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1-4: Receiver for multicarrier signals comprising FFT synchronisation circuit for locating a boundary of the guard interval;
5-7,10-24: functions performed by the FFT processor;
8,9,27-35: channel estimation and correction
25,26: BCH decoder

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1 – 4

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

information on patent family members

Inter onal Application No
PCT/US 97/18911

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